

*All the documents from this web site are intellectual property of the authors. These documents may be freely used for personal purposes and can be used for public presentation only with permission of the authors. The publications until the year 2007 were created in the Department of Electronics and Signal Processing.*     [\[2016\]](#) [ [2015](#) ] [ [2014](#) ] [ [2013](#) ] [ [2012](#) ] [ [2011](#) ] [ [2010](#)

] [ [2009](#)

] [ [2008](#)

] [ [2007](#)

] [ [2006](#)

] [ [2005](#)

] [ [2004](#)

] [ [2003](#)

] [ [2002](#)

] [ [2001](#)

] [ [2000](#)

] [ [1999](#)

] [ [1998](#)

] [ [1997](#)

] [ [1995](#)

] [ [1994](#)

]

[ [Other publications / invited talks](#)

]

## 2016

- PFEIFER, P., VIERHAUS, H. T. : "Test and Error Correction in a Dependable Wireless Communication System"; 15th Biennial Baltic Electronics Conference (BEC2016), Tallinn,

October 3-5, 2016, ISBN: 978-1-5090-1393-7/16; DOI: 10.1109/BEC.2016.7743735

- PFEIFER, P., VIERHAUS, H. T. : "FPGAs Gettin' Teeny! What Can We Expect From Them? - Field of Reliability", [DASS2016](#) , Cottbus, May 2016, published under [Fraunhofer-Institut für Integrierte Schaltungen IIS](#)

- NOVAK O., JENICEK J., ROZKOVEC M. : "Sequential Test Decompressors with Fast Variable Wide Spreading", [DDECS2016](#) , Kosice, Slovakia, April 2016

- PFEIFER, P., GLEICHNER CH., VIERHAUS, H. T. : "Flexible Test, Error Detection and Correction in Dependable Communication Systems incl. Results on 28 nm Xilinx and Altera FPGAs", [DDECS2016](#) , Kosice, Slovakia, April 2016, ISBN: 978-80-8086-256-5

- PFEIFER, P.: "FPGAs Gettin' Teeny! What Can We Expect From Them? - Field of Cryptography", [TRUDEVICE TS 2016](#) , Switzerland, April 2016

- PFEIFER, P., KACZER, B. : "AMBRAMs - An Analysis Tool, Method and Framework For Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGAs", [ERMAVS](#)

-: Workshop on Early Reliability Modeling for Aging and Variability in Silicon Systems, Dresden, Germany, March 2016

- PFEIFER, P.: "RESECU\_4\_AMBRAMs - ReSecu4 AMBRAMs - Towards Increased Reliability and Hardware Security on Modern Nanoscale FPGAs", Ubooth at [DATE2016](#) , Dresden, Germany, March 2016

## □ 2015

- CVEK, P.: "Online reconfigurable SoC with GNU/Linux", DCPS Annual Workshop 2015, Cottbus, Germany, November 27<sup>th</sup>, 2015, pp.42-47

- HUNEK, M.: "Anthropometric Measurements of Hollow Bone Structures based upon Computer Assisted Tomography", DCPS Annual Workshop 2015, Cottbus, Germany, November 27<sup>th</sup>, 2015, pp. 48-49

- PFEIFER, P.: "Towards Dependability and Security of Modern SoC Using A<sub>m</sub>BRAM<sup>s</sup> – An Advanced Set of Methods and Tools on Modern Nanoscale FPGAs",

[MEDIAN Finale 2015](#)

, Tallinn, Estonia, November 2015

- PFEIFER, P.: "A<sub>m</sub>BRAM<sup>s</sup> - An Analysis Tool, Method and Framework for Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGAs", 25th International Conference on Field Programmable Logic and Applications ( [FP L'15](#)

), London, Great Britain, September 2015, ISBN 978-0-9934-2800-5, pp. DOI: 10.1109/FPL.2015.7293963

- CVEK, P.: "Operační systém na dynamicky rekonfigurovaných procesorech", [PAD2015](#) , ISBN 978-80-7454-522-1, pp. 60-68

- PFEIFER, P.: "Modern Nanoscale FPGAs for dependable systems – new features and

- advanced measurements", [MEDIAN ISTS 2015](#) , Prague, Czech Republic, July 2015
- PLIVA, Z.: "Electronics beyond Moore", [MEDIAN ISTS 2015](#) , Prague, Czech Republic, July 2015
  - PFEIFER, P., PLIVA, Z.: "On Utilization of BRAM in FPGA for Advanced Measurements in Mechatronics", 12th International Workshop of Electronics, Control, Measurement, Signals and their application to Mechatronics [ECMSM2015](#) , Liberec, June 2015
  - SIEBER, L., PFEIFER, P. "An intelligent measurement workplace with remote control and data processing framework (Intelligentní měřicí pracoviště se systémem dálkové správy a zpracování dat)", [SKFM2015](#) , Liberec, June 2015
  - NOVAK O., JENICEK J., ROZKOVEC M. : "LFSR Reseeding Based Test Compression Respecting Different Controllability of Decompressor Outputs", 18th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems [DDECS2015](#) , Belgrade, Serbia, April 2015
  
  - NOVAK O., JENICEK J., ROZKOVEC M. : "Test Compression for Circuits with Multiple Scan Chains", 16th Latin-American Test Symposium [LATS2015](#) , Puerto Vallarta, Mexico, March 2015
  - PFEIFER P. "An FPGA lab-on-chip: An Analysis Tool and Framework for Advanced Measurements and Reliability Assessments on Modern Nanoscale FPGA", UBooth at [DA TE 2015](#) , Grenoble, France, March 2015
  
  - PFEIFER P., RAIK J., JENIHHIN M., UBAR R., PLIVA Z.: "Measuring and Identifying Aging-Critical Paths in FPGAs", [MEDIAN Workshop](#) at [DATE2015](#) , Grenoble, France, March 2015

## 2014

- DRAHONOVSKY T., M. ROZKOVEC, O. NOVAK: "A highly flexible reconfigurable system on a Xilinx FPGA," International Conference on ReConFigurable Computing and FPGAs (ReConFig 2014), 8-10 December 2014, ISBN 978-1-4799-5943-3
- PFEIFER P.: Advanced measurements and reliability assessments in modern nanoscale FPGAs, invited talk, ICTDS2014, Rakvere, Estonia, December 2014
- DRAHONOVSKY, T.: Hardware task relocation on a Xilinx FPGA, 2014, Annual DCPS Evaluation Workshop, November 2014, Cottbus, Germany, pp. 35-38
- PFEIFER P.: Reliability Assessment and Advanced Measurements In Modern Nanoscale Programmable Technologies: 28nm FPGAs Under Extreme Conditions, ZUSYS, Cottbus, Germany, November 2014
- PFEIFER, P.: Towards Increased Reliability and Hardware Security using Advanced Measurements and Data Processing on Modern Nanoscale FPGAs, (to appear: September 2014), Joint MEDIAN&TRUDEVICE Open Forum, 30 September 2014, Amsterdam, The Netherlands
- PFEIFER, P., PLIVA, Z.: A New Method for In-Situ Measurement of Parameters and Degradation Processes in Modern Nanoscale Programmable Devices. Journal Microprocessors and Microsystems, Special Issue, MICPRO2135, Elsevier, May 2014, [DOI: 10.1016/j.micpro.2014.04.008](#)

- PFEIFER, P., KACZER, B., PLIVA, Z.: A Reliability Lab-on-chip Using Programmable Arrays, 52nd IEEE International Reliability Physics Symposium, Hawaii, USA, 2014, DOI: 10.1109/IRPS.2014.6861123
- Drahoňovský, T.: Reconfigurable system on Xilinx FPGA with low memory requirements for partial bitstreams storing, 2014, 3rd Biannual European – Latin American Summer School on Design, Test and Reliability, April 2014, Frankfurt (Oder), Germany, pp. 115-119
- NOVÁK, O., J. JENÍČEK, M. ROZKOVEC. "Test-Data Compression with Low Number of Channels and Short Test Time" Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2014 IEEE 17th International Symposium., pp.104-109, 22-25 April 2014.
- PFEIFER, P., PLIVA, Z.: On Reliability Enhancement Using Adaptive Core Voltage Scaling and Variations on TSMC 28nm LP process FPGAs, The Third Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'14) Dresden, Germany, March 28, 2014
- PFEIFER, P., KACZER, B., WECKX, P., PLIVA, Z.: On Reliability Enhancement Using Adaptive Core Voltage Scaling And Variations On Nanoscale FPGAs, 15th IEEE Latin American Test Workshop, Fortaleza, Brazil, March 2014, DOI: 10.1109/LATW.2014.6841917

## 2013

- DRAHOŇOVSKÝ, T.: Víceprocesorový rekonfigurovatelný systém na obvodu FPGA, 2013, Počítačové architektury & diagnostika (PAD), September 2013, Klášter Teplá, Czech republic, pp. 75-80, ISBN 978-80-261-0270-0
- CVEK, P.: Jádru Linux a dynamicky rekonfigurovatelná platforma s procesory Microblaze, 2013, Počítačové architektury & diagnostika (PAD), September 2013, Klášter Teplá, Czech republic, pp. 129-135, ISBN 978-80-261-0270-0
- PFEIFER, P., PLIVA, Z.: On Measurement of Parameters of Programmable Microelectronic Nanostructures Under Accelerating Extreme Conditions. In: 23rd International Conference on Field Programmable Logic and Applications (FPL'13) Porto, Portugal, September 2013, IEEE 978-1-4799-0004-6/13, IEEE Catalog No. CFP13623-ART.
- PFEIFER, P., PLIVA, Z., SCHOLZEL, M., KOAL, T., VIERHAUS, H.T.: On Performance Estimation of a Scalable VLIW Soft-Core on Altera and Xilinx FPGA platforms. In: Proceedings of the 18th International Conference Applied Electronics 2013 (AE2013). Pilsen, Czech Republic, September 2013, IEEE Conference Record #30244, IEEE Catalog Number CFP1369A-PRT (Print), CFP1369A-ART (Online), ISBN 978-80-261-0166-6 (Print), ISBN 978-80-261-0165-9 (Online), ISSN 1803-7232 (Print), ISSN 1805-9597 (Online), pp. 209-212
- CVEK, P.; DRAHOŇOVSKÝ, T.; ROZKOVEC, M.: GNU/Linux and Reconfigurable Multiprocessor FPGA Platform. In: Proceedings of 11th International Workshop on Electronics, Control, Measurement, Signals and their application in Mechatronics (ECMSM2013), Toulouse, France, June 2013, IEEE Catalog Number: CFP13ECN-USB ISBN: 978-1-14673-6297-9
- PFEIFER, P., PLIVA, Z.: Investigating Diachrony of Programmable Microelectronic Nanostructures. In: Proceedings of the 11th IEEE International workshop on Electronics, Control, Measurement and Signals (ECMSM2013). Toulouse, France, June 2013, IEEE Catalog

Number: CFP13ECN-USB ISBN: 978-1-14673-6297-9, pp.26-28

- DRAHONOVSKÝ, T., ROZKOVEC, M., NOVAK, O.: Relocation of reconfigurable modules on Xilinx FPGA. . In: Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). Karlovy Vary, Czech Republic, April 2013, IEEE Catalog Number: CFP13DDE-USB, ISBN: 978-1-4673-6134-7, pp. 175-180.

- PFEIFER, P., PLIVA, Z., SCHOLZEL, M., KOAL, T., VIERHAUS, H.T.: On Performance Estimation of a Scalable VLIW Soft-Core in XILINX FPGAs. In: Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). Karlovy Vary, Czech Republic, April 2013, IEEE Catalog Number: CFP13DDE-USB, ISBN: 978-1-4673-6134-7, pp. 181-186.

- CHLOUPEK, M., JENICEK, J., NOVAK, O. ROZKOVEC, M.: Test Pattern Decompression in Parallel Scan Chain Architecture. In: Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). Karlovy Vary, Czech Republic, April 2013, IEEE Catalog Number: CFP13DDE-USB, ISBN: 978-1-4673-6134-7, pp. 219-223.

- HNILICKA, O.: FPGA Architecture for Fast Floating Point Matrix Inversion Using Uni-dimensional Systolic Array Based Structure. In: Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). Karlovy Vary, Czech Republic, April 2013, IEEE Catalog Number: CFP13DDE-USB, ISBN: 978-1-4673-6134-7, pp. 267-270.

## 2012

- PFEIFER, P., PLÍVA, Z.: Delay-Fault Run-Time XOR-less Aging Detection Unit Using BRAM in modern FPGAs. In: 13th Biennial Baltic Electronics Conference, Tallinn, Estonia, October 2012, IEEE Catalog Number: CFP12BEC-CDR, ISBN: 978-1-4673-2772-5 (Proceedings,book), ISBN: 978-1-4673-2773-2 (CDR), ISSN: 1736-3705, p.81-84

- PFEIFER, P., PLÍVA, Z.: Diachrony of programmable nanostructures. In: proceedings of the ZUSYS Dependable Systems workshop, Cottbus, Germany, October 2012, p.78-83

- CVEK P.: Jádro Linux a dynamickou rekonfigurovatelní platforma s procesory MicroBlaze. In: Počítačové architektury & diagnostika (PAD2012), September 2012, Milovy, Czech republic, pp. 35-41, ISBN 978-80-01-05106-1

- DRAHOŇOVSKÝ, T.: Návrh rekonfigurovatelného víceprocesorového systému na FPGA obvodu. In: Počítačové architektury & diagnostika (PAD2012), September 2012, Milovy, Czech republic, pp. 85-90, ISBN 978-80-01-05106-1

- PFEIFER, P., PLÍVA, Z.: Diachrony of programmable nanostructures. In: Počítačové architektury & diagnostika (PAD2012), September 2012, Milovy, Czech republic, ISBN:978-80-01-05106-1, p.121-126

- PFEIFER, P., PLÍVA, Z.: Diachrony of programmable nanostructures [poster], DMA2012, Dresden, Germany, September 2012

- PFEIFER, P., PLÍVA, Z.: On measurement of impact of the metallization and FPGA design to the changes of slice parameters and generation of delay faults. In: 22nd International

Conference on Field Programmable Logic and Applications (FPL), 2012, Oslo, Norway, August 2012, E-ISBN: 978-1-4673-2255-3, Print ISBN: 978-1-4673-2257-7, Digital Object Identifier: 10.1109/FPL.2012.6339167, p. 743-746

- ROZKOVEC, M., JENÍČEK, J., PLÍVA, Z.: Using deterministic test vectors to test FPGA circuit. In: The First Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'12), Annecy, France, June 2012, pp. 37-40

- ROZKOVEC, M.; JENÍČEK, J.; NOVÁK, O., "An evaluation of the application dependent FPGA test method," Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2012 IEEE 15th International Symposium on , vol., no., pp.22,25, 18-20 April 2012, Tallinn, Estonia, ISBN: 978-1-4673-1187-8

- CHLOUPEK, M.; NOVÁK, O.; JENÍČEK, J.: On test time reduction using pattern overlapping, broadcasting and on-chip decompression. In: Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS). Tallin, Estonia, April 2012, ISBN 978-1-4673-1187-8 , pp.300-305

## 2011

- JENÍČEK, J.; ROZKOVEC, M.; NOVÁK, O.: Test Vector Overlapping Based Compression Tool for Narrow Test Access Mechanism, 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, Cottbus, pp. 387-392, ISBN 978-1-4244-9753-91

- J. Jeníček, O. Novák and M. Chloupek, "Advanced scan chain configuration method for broadcast decompressor architecture," *Design & Test Symposium (EWDTS), 2011 9th East-West* , Sevastopol, 2011, pp. 140-143, ISBN 978-1-4577-1957-8

- DRAHOŇOVSKÝ, T.: Využití částečné dynamické rekonfigurace pro testování a zvyšování spolehlivosti FPGA obvodů, 2011, Počítačové architektury & diagnostika (PAD), September 2011, Stará Lesná, Slovakia, pp. 55-60, ISBN 978-80-227-3552-0

- PFEIFER, P.: Fault-tolerance and testability of programmable devices in safety applications with increased lifetime and reliability requirements", Počítačové architektury & diagnostika (PAD), September 2011, Stará Lesná, Slovakia, pp.14-19, ISBN 978-80-227-3552-0

- PFEIFER, P. "Fire detection safety system communication loop card with link layer coprocessor, A crossplatform version for EN54/UL864 safety systems with power and communication control signals distributed over the same pair of wires.", 10th International Workshop on Electronics, Control, Measurement and Signal (ECMS) 2011, ISBN: 978-80-7372-781-9, pp. 87-92

- DRAHOŇOVSKÝ, T.: Implementace kytarových efektů v obvodu FPGA. Sdělovací technika, pp. 4-7, 2011, ISSN 0036-9942

- DRAHOŇOVSKÝ, T., ROZKOVEC, M.: Guitar effects implementation in the FPGA circuits, 2011, Electronics, Control, Measurement and Signals (ECMS), June 2011, Liberec, Czech republic, Informal proceedings of the ECMS 2011, pp. 80-86, ISBN 978-80-7372-781-9

## 2010

- ROZKOVEC, M.; JENÍČEK, J.; NOVÁK, O.: Application dependent FPGA testing method, 13th EUROMICRO Conference on Digital System Design, Lille, pp. 525-530, ISBN:978-0-7695-4171-6
- ROZKOVEC, M.; JENÍČEK, J.; NOVÁK, O.: Application dependent FPGA testing method using compressed deterministic test vectors, On-Line Testing Symposium (IOLTS), 2010 IEEE 16th International Proceedings, Corfu, pp. 192-193, ISBN:978-1-4244-7722-7

## 2009

- ROZKOVEC, M., NOVÁK, O.: Structural test of programmed FPGA circuits, Proceedings of the 2009 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2009, Liberec, art. no. 5012114, pp. 136-139, ISBN:978-1-4244-3339-1
- JENÍČEK, J., NOVÁK, O.: COMPAS - Advanced Test Compressor, Proc. of IEEE East-West Design & Test Symposium, EWDTs 2009, Moscow, pp. 532-537

## 2008

- Novák, O., Jeníček, J.: Test Pattern Overlapping - a Promising Compression Method for Narrow Test Access Mechanism SOC Circuits, Radioelectronics & Informatics, No. 1, pp. 26-33, 2008, ISSN 1563-0064
- JENÍČEK, J.: Nový kompresní algoritmus pro systém COMPAS. Proc. of PAD 2008,

September 2008, Hejnice, Czech, pp. 81-88, ISBN 978-80-7372-378-1

- ROZKOVEC, M.: Koncept rekonfigurovatelné testovací architektury pro FPGA obvody. Proc. of PAD 2008, September 2008, Hejnice, Czech, pp. 37-44, ISBN 978-80-7372-378-1

- JENÍČEK, J.: Efficient Test Pattern Compression Method Using Hard Fault Preferring. Proc. of DSD 2008, September 2008, Parma, Italy

- ROZKOVEC, M.: Implementation of Dynamically Reconfigurable Test Architecture for FPGA Circuits. Proc. of DDECS 2008, April 2008, Bratislava, Slovakia, pp.182-185, ISBN 978-1-4244-2276-0

- NOVÁK, O., PLÍVA, Z., JENÍČEK, J., MADER, Z., JARKOVSKÝ, M.: Self-Testing SoC with Reduced Memory Requirements and Minimized Hardware Overhead. Acta Electrotechnica et Informatica, Vol. 8, No. 1, pp. 22-32, 2008, ISSN 1335-8243

## **2007**

- JENÍČEK, J.: Použití algoritmu COMPAS s různými ATPG, Proc. of PAD 2007, pp. 27-32, ISBN 978-80-7043-605-9

- PLIVA Z., KOLAR M., DOSEK P., SLUKA T.:A Piezoelectric elements and their electronics driving with help of FPGA circuits, Taylor&Francis, Jun 12. 2007, Journal Ferroelectrics 351:1, pp.187 - 195, ISSN: 1521-0464

- JENICEK J., NOVAK O.:A Test Pattern Compression Based on Pattern Overlapping, Proc. of DDECS 2007, Apr. 2007, Krakow, Poland, pp.29 - 34, ISBSN: 1-4244-1161-0

## **2006**

- GOYAL A., SARKAR A., PLIVA Z., KOSTAKOVA E., LUKAS D.:Designed Electric Circuit Used as Collector for Electrospinning, Proc. of Strutex 2006, Liberec, Czech, Nov.2006, pp.641-646. ISBN 80-7372-135-X

- NOVÁK, O., PLÍVA, Z., JENÍČEK, J., MADER, Z., JARKOVSKÝ, M.: Self Testing SoC with Reduced Memory Requirements and Minimized Hardware Overhead. Proceedings of DFT2006, Arlington, USA, October 2006, pp. 300-308, ISBN 0-7695-2706-X



- JENÍČEK, J.: Optimalizace kompresního systému kompas. Proc. of PAD 2006, Papradno, SK, pp. 77-82, ISBN 80-969202-2-7

## 2005

- NOVÁK, O., GRAMATOVÁ, E., UBAR, R. and coll.: Handbook of testing electronic systems. Nakladatelství ČVUT, srpen 2005, 395 stran, ISBN 80-01-03318-X
- NOVÁK, O., ZAHRÁDKA, J., PLÍVA, Z.: COMPAS - Compressed Test Pattern Sequencer for Scan Based Circuits. EDCC2005, Lecture Notes in Computer Science 3463, pp. 403-414, Springer-Verlag 2005, ISSN 0302-9743
- PLÍVA, Z., NOVÁK, O., SIEKIERSKA, K., GRODNER, M.: Test\_Access block - Serial Scan vs. Random Access Scan. proceedings of MIXDES2005, Krakow, Poland, June 2005, pp. 861-865, ISBN 83-919289-9-3
- PLÍVA, Z., NOVÁK, O., SIEKIERSKA, K., GRODNER, M.: Test Access Circuit for Education. proceedings of DDECS2005, Sopron, Hungary, April 2005, pp. 27-32, ISBN 963-9364-48-7
- JARKOVSKÝ, M., PLÍVA, Z., NOVÁK, O.: Software for Test\_Access Circuit for Education. Proceedings ECMS 2005, Electronique, Cotrôle, Modélisation, Mesure et Signal, 17-20 May 2005. Toulouse: Université Paul Sabatier.
- NOVÁK, O.: Self-test in logic blocks, Why we need deterministic test pattern generation?, Tutorial of the 8th IEEE DDECS workshop, Sopron, Hungary, April 13, 2005
- NOVÁK, O.: Handbook of Testing Electronic Systems. Handouts of the Testing of Digital Systems REASON workshop, May 22, 2005 Tallinn, Estonia
- MADER, Z. : System-on-a-Chip Diagnostics Using RESPIN Architecture. In: EDCC-5, Budapest, May 2005
- JENÍČEK, J.: Optimalizace systému pro kompresi testovacích vektorů COMPAS. PAD 2005, pp. 73-76, ISBN 80-01-03298-1
- JARKOVSKÝ, M.: Uživatelské rozhraní a řídicí programové vybavení pro diagnostiku SoC obvodů s využitím RESPIN architektury. Počítačové architektury & diagnostika 2005 (PAD 2005), str.61-65, 21.- 23.9.2005, Lázně Sedmihorky. ISBN 80-01-03298-1
- PĚNIČKA, J., DOŠEK, P.: Neural networks from Matlab to FPGA circuit. In: 7th International Workshop on Electronics, Control, Modeling, Measurement and Signals, CD proceedings, May 17-20, 2005, Toulouse, France
- RICHTER, A. - RYDLO, P. - PUSTKA, M. - KOLÁŘ, M.: Pulse Driving of Piezoceramic Actuators and Their Present Technical Limitations. Ferroelectrics, Volume 320, 2005, p. 125-132
- SVOBODA P.: DirectShow camera framework for Delphi. In: Mechatronika 2005, FM TnU AD Trenčianské Teplice, Slovensko, květen 2005, s. 77-80. ISBN 80-8075-058-0

## 2004

- DOLEŽAL, I.: Low-Cost High-Resolution Quartz Thermometer. In: Digest of Technical Papers, EUROSENSORS XVIII, Řím, září 2004, s. 760-761.
- DOŠEK, P.: Mathematical operations in FPGA circuits. In: International Workshop Digital Technologies 2004, Žilina, Slovak Republic, December 2004, pp. 5.-10, ISBN 80-8070-334-5
  
- DOŠEK, P.: Matematické operace v FPGA obvodech. K<sup>7</sup>, FM TUL, Liberec 2004, č. 4, str. 11-16, ISSN 1214-7370
- MADER, Z.: Diagnostika SoC obvodů s využitím RESPIN architektury. In: Seminář PAD, Moravany nad Váhom, Slovak Republic, Sept. 2004, ISBN 80-969202-0-0, s. 66-71.
- NOVÁK, O., ZAHŘÁDKA, J., HOLUBEC, M., JENÍČEK, J.: Test Set Compaction and Compression for circuits with Scan. Informal Digest of Papers of the IEEE European Test Symposium, Ajaccio Corsica, France, 2004, pp. 13-14.
- RICHTER, A., PUSTKA, M., RYDLO, P., KOLAR, M.: The computation of traveling-wave velocity on the stator surface and excitation by PWM modulation with higher harmonic suppression. *Ceramics International*, Volume 30, Issue 7 , 2004, p. 1857-1861.
- RICHTER, A., RYDLO, P., PUSTKA, M., KOLÁŘ, M.: Pulse driving of piezoceramic actuators and their present technical limitations. In: ECAPD7, Liberec, September 2004
- ZAHŘÁDKA, J.: Optimalizace systému pro kompresi testovacích vektorů COMPAS, In: Seminář PAD, Moravany nad Váhom, Slovak Republic, Sept. 2004, ISBN 80-969202-0-0, s. 78-82.
- NOVAK O., PLIVA Z., NOSEK J., HLAWICZKA A., GARBOLINO T., GUCWA K., : Test-Per-Clock Logic BIST with Semi-Deterministic Test Patterns and Zero-Aliasing Compactor, Kluwer Academic publishers - *Journal of Electronic Testing: Theory and Applications* 20, ISSN 0923-8174, pp.109-122, 2004
- PLIVA Z.,: Practical Teaching of the Test Access, proceedings of BEC2004, Oct. 2004, Tallinn, Estonia, pp.263-264, ISBN 9985-59-462-2
- DOLEŽAL, I., VONDRA, R., GROSMAN, J.: Optické snímání plošné hustoty rouna na mykacím stroji [Sborník technických zpráv VC Textil, sekce C, oblast Zlepšení parametrů mykacího stroje], 18 str., ISRN TUL - VCT/C - MŘTP --04/001/CZ, Liberec, TUL 2004.
- DOLEŽAL, I., SVOBODA, P.: Detekce barevných vad v přízi [Zpráva o činnosti ve Výzkumném centru Textil Liberec, Sekce C], 4 str., Liberec, TUL 2004
- HES, L., DOLEŽAL, I., RICHTER, A.: Způsob bezkontaktního měření povrchové teploty a/nebo emisivity objektů a zařízení k provádění způsobu. PV 2004-137 z 27.1.2004, přihláška vynálezu
- NOVAK, O., PLIVA, Z.: Tutorial Additional Hardware for IC Testability Improvement, April 18, 2004, DDECS04, Design for Testability and BIST
- PLIVA, Z.: Tutorial Advanced Methods of Testing Electronics Systems v Sofii, May 29,

2004, SOC testing

- PLIVA, Z.: Tutorial Advanced topics of SOC design and test, Oct 5, 2004, BIST in SoC

## 2003

- DOLEŽAL, I.: A Low-Cost Flexible Sound Signal Generator for Embedded Microcomputers. Proc. of 6th Workshop on Electronics, Control, Measurement and Signal (ECMS '03), June 2-4, 2003, Liberec, pp. 21-25, ISBN 80-7083-708-X
- NOVAK, O.: Comparison of test pattern decompression techniques. Proc. Design Automation and Test in Europe conference DATE03, Munich, March 3-7, 2003, pp. 1182-1183, ISBN 0-7695-1870-2, ISSN 1530-1591
- NOVAK, O.: Efficiency of test pattern decompression Techniques. Radioelectronics & Informatics 1003 / 3, ISSN 1563-0064, pp. 19-22
- NOVAK, O.: Easy testable design and BIST. Radioelectronics & Informatics 1003 / 3, ISSN 1563-0064, pp. 205.
- RICHTER, A., RYDLO, P., KOLÁŘ, M.: Ultrasonic Piezoceramics Motor Driven by PWM Modulation with Higher Harmonic Suppression. In: ICMAT 2003 International Conference on Materials for Advanced Technologies), 7. - 12. December 2003, Singapore
- PLIVA, Z., NOVAK, O., NOULLET, J., L.: Comparison of the Low-Power Diagnostics Methods, proceedings of ECMS 2003, June 2-4, 2003, Liberec, pp. 299-304, ISBN 80-7083-708-X (Random Access Scan - RAS, pdf: [175kB](#) )
- ZAHRADKA, J., HOLUBEC, M., NOVAK, O.: COMPAS - System for Finding of a Compress Test Pattern Sequence. Proc. of ECMS'03, Liberec, June 2003
- NOVAK, O., ZAHRADKA, J.: Test Pattern Decompression Technique for Circuits with Scan. Proc. of IEEE ETW 2003, Maastricht, Netherlands, May 2003, pp. 103-104
- PLIVA, Z., NOVAK, O.: Scan Based Circuits with Low Power Consumption, Proc. of DDECS2003, April 14-16, 2003, Poznan, pp. 267-232, ISBN 83-7143-557-6 (Random Access Scan - RAS, pdf: [161.3kB](#) )

## 2002

- PLIVA, Z., NOVAK, O.: Low power Boundary Scan Design, Proc. of BEC2002, October

6-9, 2002, Tallinn, pp. 265-268, ISBN 9985-59-292-1 (Random Access Scan - RAS, pdf: [95.3kB](#))

[1](#)

- PLIVA, Z., NOVAK, O., BOURDEU d'AGUERRE, P.: Hardware Overhead of Boundary Scan and RAS Design Methodologies, Proc. of DDECS2002, April 17-19, 2002, Brno, pp. 36-43, ISBN 80-214-2094-4 (Random Access Scan - RAS, pdf: [238.2kB](#))
- NOVAK, O., DOLEZAL, I.: Microprocessor-Based Controllers and Microelectronics. In Bishop R. H. (ed.) : The Mechatronics Handbook. Boca Raton : CRC Press, 2002, s. 4-1-7. ISBN 0-8493-0066-5

## 2001

- PLIVA, Z., NOVAK, O., BOURDEU d'AGUERRE, P.: Hardware Overhead of BIST Equipment, Proc. of AE2001, Sept 2001, Pilsen, pp. 204-207, ISBN 80-7082-758-0
- PLIVA, Z.: Built-In Self Test From Hardware Point of View, Proc. of ECMS-2001, May 2001, Toulouse (Fr), pp. 131-135, ISBN 80-7083-444-7
- NOVAK, O., NOSEK, J.: Test-per-Clock Testing of the Circuits with Scan , Proc. of 7th IEEE International On-Line Testing Workshop, July 2001, Taormina, Italy
- NOVAK, O., HLAWICZKA, A., GARBOLINO, T., GUCZWA, K., PLIVA, Z., NOSEK, J.: Low Hardware Overhead Deterministic Logic BIST with Zero-Aliasing Compactor. Proc. IEEE DDECS conf. Győr (Hungary), Apr. 2001 ( [183.3kB](#) )
- DOLEZAL, I.: Přístroj P-TEST. [Dílčí zpráva VC Textil], ISRN-TUL-TZ/MS-00/001/CZ, Liberec, TUL 2001.

## 2000

- NOVAK, O., HLAVICKA, J.: An Efficient Deterministic test Pattern Compaction Scheme Using Modified IC Scan Chain. Proc. of IEEE European Test Workshop (ETW'00), Lisbon (Portugal) 25-28.5.2000, pp. 305-306 ( [92.5kB](#) )
- NOVAK, O., NOSEK, J.: On Using Deterministic Test Sets in BIST. Proc. of 6th IEEE International On-Line Testing Workshop, 3-5. July, 2000, Palma de Mallorca, Spain, pp.

127-132, ISBN 0-7695-0646-1( [72.5kB](#) )

- NOVAK, O., HAJEK, D., NOSEK, J.: Optimised Hardware Test Pattern Generator for BIST. Proc. of Design and Diagnostics of Electronics Circuits and System Workshop, April 5-7, 2000, Smolenice, Slovakia, pp. 205- 208, ISBN 80-968320-3-4
- PLIVA, Z., NOVAK, O.: Practical Experience with Design of Cellular Automaton in CADENCE.Proc. of Design and Diagnostics of Electronics Circuits and System Workshop, April 5-7, 2000, Smolenice, Slovakia, pp. 217- 218, ISBN 80-968320-3-4
- DOBIASOVA, J.: Analyza vlivu pusobicich na kvalitu vyroby desek s plosnymi spoji v podniku CUBECZ. ISRN-TUL-KES-T-PZ-00-002-C1-CZ, listopad 2000, 15 stran
- NOSEK, J.: Generovani testovacich vektoru zalozene na celularnim automatu. ISRN-TUL-KES-T-PZ-00-001-C1-CZ, listopad 2000, 20 stran
- PLIVA, Z.: Navrh snadno testovatelných obvodu. Vyzkumna zprava ISRN-TUL-KES-T-PZ-00-006-C1-CZ, listopad 2000, 10 stran
- NOVAK, O., RYDLO, P., DOLEZAL, I., KOLAR, M., PLIVA, Z.: Krystalovy teplomer.Vyzkumna zprava ISRN-TUL-KES-T-PZ-00-007-C1-CZ, listopad 2000, 23 stran
- NOVAK, O.: IC Design and Diagnostics Group Research Activities.Proc. of Computer Science Education Workshop (CSEW2000), Liblice, Nov. 2000, pp. 70-75, ISBN 80-01-02264
  
- PLIVA, Z., NOVAK, O., KOLAR M.: Designing of BIST equipment in Cadence, proc. of Computer Science Education Workshop (CSEW2000), Liblice, Nov. 2000, pp. 70-75, ISBN80-01-02264-1

## 1999

- NOVAK, O.: Pseudorandom, Weighted Random and Pseudoexhaustive Test Patterns Generated in Universal Cellular automata. Springer: Lecture Notes in Computer Science 1667 pp.303-320, ISSN0302-9743, ISBN 3-540-66483-1, September 1999 ( [150.6kB](#) )
- NOVAK, O.: Weighted Random Patterns for BIST Generated in Cellular Automata. Proc. of 5.th IOLTW, Rhodes, Greece, July 1999, pp. 72-76 ( [56.2kB](#) )
- NOVAK, O.: Random Pattern Coverage Enhancement for BIST. Comp. of papers of ETW'99 Constance, Germany, May 1999, 2 pp. ( [27kB](#) )
- NOVAK, O.: Codes with Improved Properties Generated in Linear Feedback Shift Registers and Cellular Automata. Proc. of ECMS'99 Liberec, May 1999, pp.108-113 ISBN 80-7083-339-4
- DOLEZAL, I.: Modemless Phone Dialer Using PC COM Port.In: Proc. of IV. Workshop on Electronics, Control, Measurement and Signals (ECMS '99), TU Liberec, May 1999, s.135-138, ISBN 80-7083-339-4
- PLIVA, Z.: ASIC Design, prubezna zprava, Liberec, dec. 1999, ISRN TUL-KES-TZ/PZ-99/001/C1-CZ

## 1998

- NOVAK, O.: Design of Cellular Automaton for Built-in Deterministic Testing. Proc. of DDECSW, Szczyrk, Poland, September 1998, pp.161-166, ISBN 83-908409-6-0
- NOVAK, O., HLAVICKA, J.: Design of a Cellular Automaton for Efficient Test Pattern Generation. Proc. IEEE ETW 1998, Barcelona, Spain, pp. 30-31
- DOLEZAL, I.: Nitrogen Cryostat Thermometer and Control Unit. Proc. of Int. Conference Programmable Devices and Systems, Gliwice, Poland, February 1998, pp. 239 -246.
- HLAVICKA J, NOVAK, O.: Methods of Pseudoexhaustive Test Pattern Generation. VUT FEL, research report DC-98-08, 27 stran

## 1997

- DOLEZAL, I.: Serial Linked Multifunctional Peripheral Device. Proc. of 3rd ECMS Workshop, Toulouse, France, June 1997, pp.199-207.
- HLAVICKA J., NOVAK, O.: Built-in Self-Test Equipment - State of the Art. Proc. of DDECS'97, Ostrava, May 1997, pp.22-34.
- NOVAK, O.: Built-in Pseudoexhaustive Test Set Generators. Proc. of 3rd ECMS Workshop, Toulouse, France, June 1997, pp.145 -149.

## 1996

- NOVAK, O.: Enhancing Pseudoexhaustive Test Set Quality by Code Bit Inversions. Proc. of IEEE ETW 1996, Montpellier, France, 1996.
- NOVAK, O.: Pseudoexhaustive Test Set Generators for FPGAs. Proc. of International

conference on programmable devices and systems PDS '96. VŠB TU Ostrava, November 1996, pp. 55-61, ISBN 80-85988-12-7

- HLAVICKA, J., NOVAK, O.: Enhancing Pseudoexhaustive Test Set Quality by Code Bit Inversions. Proc IEEE ETW96, Montpellier, France, June 1996

## **1995**

- NOVAK, O., HLAVICKA, J.: Enhancing Fault Coverage of Pseudoexhaustive Test Sets. Proc. of 1st.IEEE International On-Line Testing Workshop, Nice France, 1995, s.173-177

- NOVAK, O.:Pseudoexhaustive Test Sets Generated by Code Matrix Bit Inversions. Proc. Workshop on Design Methodologies for Microelectronics, Smolenice Castle, Slovakia, 11-14. 9. 1995, pp. 285-286

- NOVAK, O.: Pseudoexhaustive Test Set Optimization Using Weak Representations. Proc. DDECS'95 Ostrava, 19-21.9. 1995 pp. 39-43.

- DOLEZAL, I.: A Low-Cost Flexible Sound Signal Generator for Embedded Microcomputers. In: Proc. of VI. Workshop on Electronics, Control, Measurement and Signals (ECMS '03), TU Liberec, June 2003, pp.21-25, ISBN 80-7083-708-X

- DOLEZAL, I., Hes, L.: P-TEST - Computerized Instrument for Testing of the Water Vapour and Thermal Resistance of Fabrics. In: CD Proc. of 2003 IEEE International Symposium on Industrial Electronics, Rio de Janeiro, Brazil, June 2003, 5 pages, ISBN 0-7803-7912-8

- DOLEZAL, I.: A-D Converters Module for PC. In Proc. of Programmable Devices and Systems International Conference, Gliwice, Polsko, Nov. 1995.

- DOLEZAL, I.: The A/D converters module for tensile tester/PC interface. In: Electronic Control and Measuring Systems, Liberec, TU Liberec 1995, p.16-24.

## **1994**

- DOLEZAL, I.: ALFATEST - Instrument for Measuring Thermal Properties of Walls and Building Materials (in Czech). In Proc. of Electro-Workshop'94, Liberec, 1994, pp.3-13.

- DOLEZAL, I.: Control System of Cans Operation for the Carding/Drawing Machine in Automated Spinning Mills (in Czech). In Proc. of Electro-Workshop'93, Liberec, 1994, pp.41-53.

## Other publications

- PFEIFER, P.: FPGA aging measurement and results, TUT Tallinn, Estonia, February 2013, supported by COST Action MEDIAN STSM
- PFEIFER, P.: Spolehlivost mikroelektronických obvodů a nanostruktur, CVUT Praha, invited talk, February 2012
- PFEIFER, P.: MTBF alias reliability analysis/assessment, models, failure rate estimation methods and standards, Czech Technical University Praha (CVUT), invited talk, February 2012
  
- PFEIFER, P.: Investigating diachrony of modern technologies – A new In-Situ method for complex measurements using programmable gate arrays”, IMEC, Leuven, Belgium, November 2013
- PFEIFER, P., PLIVA, Z.: "Aging effect in New Technologies: Investigating 28nm and below", Centre for Integrated Electronic Systems and Biomedical Engineering - CEBE, Electronics Aging session, Tallinn, Estonia, October 2013, av. [here](#)
- PFEIFER, P., PLIVA, Z.: "Diachrony of Programmable Nanostructures: Investigating Aging of FPGAs down to 28 nm", 26th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, invited paper, poster, New York city, NY, USA, October 2013
- PFEIFER, P.: "Diachrony of Programmable Nanostructures: Aging effect on FPGAs down to 28nm", TUL&BTU ZUSYS seminar Dependable Systems on FPGAs, Liberec, September 2013
- PLIVA, Z.: Prohlížeče Gerber dat 5 - CAMtastic!. Computer Design 02/4, pp. 44 - 47, ISSN1212-4389
- PLIVA, Z.: GC-Prevue v9.0.8. Computer Design 2000/5, pp. 56 - 57, ISSN1212-4389
- PLIVA, Z.: ECAM350 v6.0. Computer Design 2000/6, pp. 54 - 55, workshop pp. 23 - 24, ISSN1212-4389
- PLIVA, Z.: GerbTool v10.0. Computer Design 2000/5, pp. 60 - 61, workshop pp. 22, ISSN1212-4389
- PLIVA, Z.: ViewMate. Computer Design 2000/3, pp. 70 - 71, workshop pp. 22-23, ISSN1212-4389
- PLIVA, Z.: Design and Manufacturing errors and their eliminating with CAD/CAM. proc. Aplikovan elektronika 99 (AE99), Plze , Sept. 1999, ISBN 80-7082-512-X
- PLIVA, Z.: Recenze programu Eagle. Computer Design 1999/3, pp. 78 - 80, ISSN1212-4389
- PLIVA, Z.: Kam miri sipka OrCADu II. Computer Design 1998/6, pp. 86 - 89, ISSN1212-4389
- PLIVA, Z.: Kam miri sipka OrCADu. Computer Design 1998/5, pp. 64 - 68, ISSN1212-4389



- PLIVA, Z.: Zlato od Mentor Graphics - part II. Computer Design 1998/2, pp. 70 - 73, ISSN1212-4389
- PLIVA, Z.: Zlato od Mentor Graphics - part 1. Computer Design 1998/1, pp. 64 - 68, ISSN1212-4389
- PLIVA, Z.: Na Gerber a plosne, spoje s CAM350. Computer Design 1997/5, pp. 96 - 98, ISSN1212-4389
- PLIVA, Z.: Na CAD zdola. Computer Design 1997/4, pp. 106 - 108, ISSN1212-4389

800x600

Normal 0 21 false false false CS X-NONE X-NONE MicrosoftInternetExplorer4