An Efficient Deterministic Test Pattern Compaction Scheme Using Modified IC Scan Chain

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Abstract

In this paper, we propose a new scheme for Built-In Self-Test (BIST) that uses an LFSR obtained by adding feedback loops to the IC boundary scan chain. This LFSR first generates random patterns to cover easy-to-test faults and after the random testing phase it is partially loaded with seeds to generate deterministic vectors for hard-to-test faults. The seeds are obtained by solving systems of linear equations for seed variables, respecting the positions where the test patterns have specified values. The scan chain based LFSR due to its length produces sequences with very low probability of linear dependence of generated patterns. This would hardly be achievable using an added external LFSR, whose length has to be minimized due to the cost limitations. The probability of encoding a test pattern into a seed is the same as in the case of using multiple polynomial LFSR, but the hardware overhead is lower. Fault coverage for the ISCAS benchmark circuits was simulated and an optimized testing strategy for fully scanned ICs was proposed on the basis of the obtained results.

The test patterns in mixed-mode testing are obtained partially from a hardware TPG and partially from a software ATPG tool, where the hardware TPG tests the easy-to-test faults and the ATPG generated patterns detect the hard-to-test faults. We propose a scheme that instead of using a MP LFSR [1] for compaction of deterministic test patterns uses longer LFSRs partially or completely embedded into the boundary scan chain. One of possible implementations of this approach is shown in Fig.1.

The scan chain is divided into three parts. The first part which corresponds to the input boundary scan cells is converted into an LFSR. It is used for pseudorandom test pattern generation and deterministic test pattern compaction. The conversion is done by adding linear feedback loops to the respective part of the scan chain, according to a primitive or non-primitive polynomial. The feedback taps can be disconnected by the multiplexer and an arbitrarily big part at the beginning of the scan chain can be seeded from a FIFO memory. The second part of the chain which corresponds to the internal CUT flip-flops is a standard shift register, which receives the values from the LFSR. Finally, the third (output) part of the scan chain forms a data compactor. In the random pattern generation phase the patterns are generated in the LFSR and simultaneously shifted into the rest of the chain. Then the functional clock cycle is performed and the responses are stored either in the data compactor or in the internal CUT flip-flops. Next shifts accumulate signatures of all the

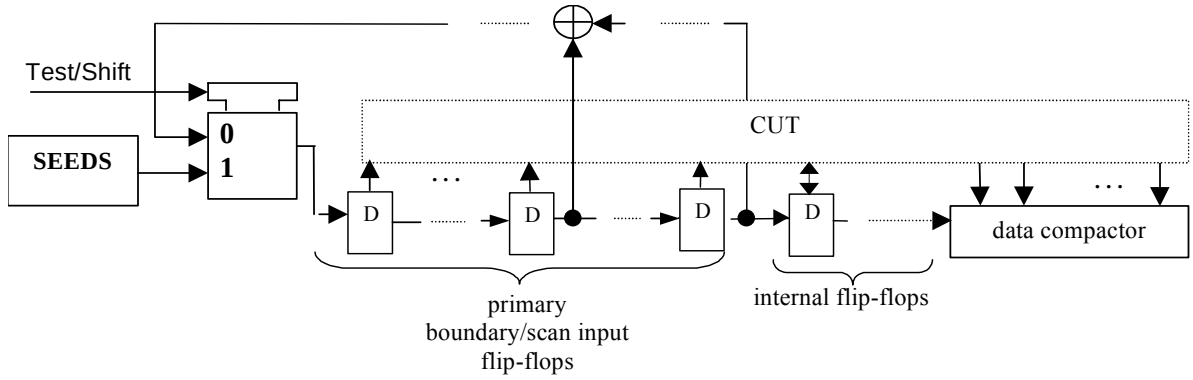

Fig. 1. Proposed mixed mode testing scheme which uses boundary scan with added feedback and partial reseeding of the LFSR

Table 1. Comparison of the obtained results with the MP LFSR method

			MP LFSR [1]				proposed method				
circuit	circuit inputs (*m*)	CUT flip-flops	degree of MP-LFSR	deterministic test patterns	LFSR polynomials	used memory	degree of LFSR	extra LFSR bits	seeded bits (*k*)	deterministic test patterns	used memory
c2670	157	0	52	77	2	4158	157	0	52	79	4108
c3540	50	0	19	1	1	19	50	0	19	1	19
c7552	206	0	145	92	8	13432	206	0	133	89	11837
s641	35	19	22	11	2	253	54	19	22	9	208
s713	35	19	22	11	2	253	54	19	22	9	208
s820	18	5	15	32	2	512	23	5	15	4	60
s832	18	5	15	33	2	528	23	5	15	4	60
s953	16	29	15	50	2	800	31	15	15	11	165
s1196	14	18	17	20	2	360	32	18	16	6	96
s1238	14	18	17	21	2	399	31	17	16	13	208
s1423	17	74	25	5	2	130	42	25	25	4	100
s5378	35	179	25	31	2	806	60	25	22	30	660
s9234	19	228	52	237	3	12561	71	50	52	237	12324
s13207	121	579	60	179	2	10919	181	60	59	179	10561
s15850	14	597	57	246	1	14022	69	55	55	242	13310
s38417	28	1632	106	795	6	85065	134	106	106	736	78016

responses in the compactor. Before each deterministic test step the flip-flops in the chain are reset. Every *k*-bit seed is shifted into the first *k* stages of LFSR, one clock cycle is then performed and the responses are captured.

We compare the hardware overhead connected with the proposed method with a simple boundary scan design. The overhead includes the XOR gates in the feedback, the feedback taps, the multiplexer and the seed memory. If the number of circuit primary inputs is too small, it is not sufficient to use only the boundary scan flip-flops for creating the LFSR and we have to add some external flip-flops in order to improve the compression ability of the TPG. In this case the hardware overhead is increased by the number of added flip-flops (In the table they are denoted as extra LFSR bits).

On the basis of theoretical evaluation of the proposed test compaction method we expected that the scheme could be effective for testing circuits with hard to test faults. We performed experiments with ISCAS 85 and ISCAS 89 benchmark circuits, which have some random resistant faults. Fault coverage in each of the benchmark circuits was initially simulated for 10 000 random patterns generated by the LFSR from Fig. 1, which performed division of the LFSR state by a chosen polynomial. After finishing the random testing phase we generated test patterns by a structural method for the random resistant faults and verified whether they can be encoded with the help of partially seeded LFSR In the table the number of seeded bits is denoted as k. In the case of the ISCAS 85 circuits (combinational circuits) we can see in the Table that the proposed method requires no extra flip-flops whereas the MP LFSR requires those extra flip-flops, which form the LFSR. In the case of the ISCAS 89 circuits the number of extra bits is chosen in such a way that the TPG hardware overhead can be considered the same as for MP LFSR. The memory volume used for seeds is both for the ISCAS 85 and 89 circuits lower than that for MP LFSR.

We can conclude that our experiments showed, that the MP LFSR method for compressing the deterministic test patterns can be replaced by simpler LFSR with partial reseeding. The proposed TPG has low hardware overhead and saves the memory for storing the seeds. It can be more easily controlled because of the fact that it is not necessary to switch between different MP LFSR polynomials.

Acknowledgement

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Reference

[1] HELLEBRAND, S. – RAJSKI ,J. - TARNICK, S.- VENKATARAMAN, S. - COURTOIS, B.: Built-In Test for Circuits with Scan Based on Reseeding of Multiple-Polynomial Linear Feedback Shift Registers. IEEE Trans. on Comp., vol. 44, No. 2, February 1995, pp. 223-233