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Comparison of the Low-Power Diagnostics Methods

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Abstract: *In this paper, we discuss possibilities of reduction of the power used for loading test patterns into a Circuit Under Test (CUT). By the term CUT we mean circuit or a module of a complex circuit, which has to be tested in one test session. There are several methods how to move test patterns into the CUT. If we speak about sequential circuits equipped with some of the diagnostic access circuitry, we usually mean by the term CUT the combinational part of the circuit only. As it is not usually possible to use the primary circuit inputs for test pattern insertion and the test patterns for complex circuits are generated in such a way that some diagnostic access to flip-flops (FF) is demanded, several diagnostic access methodologies were created.*

I. INTRODUCTION

The diagnostic access approaches can be divided into serial access methods and random access methods [12]. Historically the main representative of the serial diagnostic access methods was the method called LSSD (Level Sensitive Scan Design [5]) and the method RAS (Random Access Scan [2]) can serve us as a representative of the parallel methods. LSSD was proposed for scanning in and out the internal FF bits only. RAS could be used also for observing logical values on wires. In 1993 a new serial method called BS (Boundary Scan [3], [7]) was standardized. This method was designed so that it enables scanning in and out the circuit inputs and outputs and it can perform several other functions. During the last decade the serial diagnostic access methods became to be the most important ones within all diagnostic access methods and nowadays they are widely used. In order to further, simplify testing of sequential circuits the BS is completed with a chain of scan cells (SC), which replace internal FFs. On the contrary, to the chain of I/O BS cells the internal FF chain influences the internal combinational logic of the CUT during shifting test patterns. With growing size of the produced integrated circuits new problems occurred: Shifting test patterns in long scan chains causes unacceptably big heat dissipation, the test clock frequency has to be lowered and/or special gates avoiding signal wide spreading has to be used. This high consumption should be a problem in the novel battery powered portable devices and in the high clock frequency designs.

During the last decade serial diagnostic access methods became the most important within all diagnostic methodologies and they are widely used. These diagnostic access methods were standardized and the IEEE 1149 standard called Boundary Scan (BS) [3], [7] is used for designing complex circuits. As modern IC production technologies allow higher connectivity of the construction blocks of ICs, the following question arises: Is it necessary to use serial diagnostic access methods or could it be possible to use some parallel method? RAS was considered to be an alternative to the serial methods. It has several advantages:

- it uses simpler construction blocks,
- it allows to read a logical value from a wire without any flip-flop
- it spares energy which is necessary for reading and writing diagnostic data.

The main disadvantage of the RAS method is that it requires higher number of long connecting wires and the RAS cells are more complex than the Scan Chain. In this paper, we demonstrate our designs of ISCAS circuits [4] with different diagnostic cells, which have the same controlling signals as they are used in BS diagnostic cells. We compare the area of the original circuit with the chip area of the circuits with serial or parallel diagnostic access cells. Using the RAS diagnostic access methodology may be an alternative solution of the described problem. RAS cells are not concatenated in a chain and thus the output activity of the FFs is substantially lower. As the BS is a commonly used standard access method and it is not necessary to minimize the power consumption in all the ICs it is

useful to design a RAS like circuitry that can be used simultaneously with the BS. This approach was used in [10].

II. Boundary Scan with Scan Chain

There are several methods how to move test patterns into the Circuit Under Test (CUT). It is not usually possible to use the primary circuit inputs for test pattern insertion. Usually a multiplexor is inserted to the original data input. The second functional input of this multiplexor is connected with the diagnostic input signal and the multiplexor function is controlled by a mode signal.

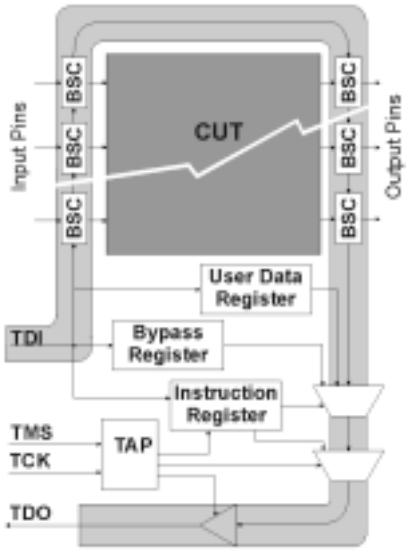

Fig. 1: Boundary Scan – the principle scheme

This method was designed so that it enables scanning in and out circuit inputs and outputs and it can be used for performing several other functions. The BS IC equipment is shown in Fig. 1. Data flow is managed by the TAP (Test Access Port) controller, which is driven by TMS (Test Mode Select) and TCK (Test Clock). The TAP controller can set each of the BSCs (Boundary Scan Cell) to the normal function – data coming from Input Pins are connected to the inputs of the CUT. In the Scan mode it is possible to send serial input data from TDI (Test Data Input) through the shift register to the relevant BSC. In reverse, it is possible to export serially all the BSC's outputs to TDO (Test Data Output). The TAP controller can also bypass the IC using the Bypass Register.

The main advantage of the serial diagnostic access methods is that they need fewer wires for controlling the diagnostic data shifting through the scan chain. A main disadvantage of this approach is that it needs two D flip-flops for every controlling and observing IC point. Another disadvantage of the serial methods occurs if we want to have a diagnostic access to internal FFs. These internal FFs can be included into the scan cells but as the FF outputs are directly connected with the rest of functional logic, shifting patterns through the scan chain (SC) causes an activity of the combinational part of the circuit. This activity could be in some cases unacceptable. One solution of the circuit activity reduction was proposed in [6]. As the solution is based on gating the FF outputs with the help of a NOR gate it causes an additional delay in critical functional path. A solution of design partitioning and reordering the scan chain was published in [13] and [9]. Another way was shown in [8]. The authors have proposed filtering of the test pattern subsequences generated in a pseudorandom pattern generator, which do not detect faults. This filtering is performed in additional combinational circuits.

III. Design of Asynchronous Random Access Scan

The main idea of the proposed solution is described in [11] (Fig. 2). After the "Reset", the address is decoded in such a way that the output of the input part of BS is connected with the first RAS cell. The address signal is used also for read enabling of the cell with the consequent address. During shifting patterns through the scan chain the RAS cells are activated according their addresses and the bits from the BS scan chain are loaded into the RAS latches. The actual values of RAS cells are captured simultaneously with loading test patterns into cells in the auxiliary FF and then loaded into the output part of the BS chain.

We have designed all the circuits in Silicon Ensemble (0.6 μm AMS technology tech-cub [1]). In this technology there is not any latch with Set and Reset inputs available, we have used D-FFs with asynchronous Set and Reset inputs instead of simple latches. If the

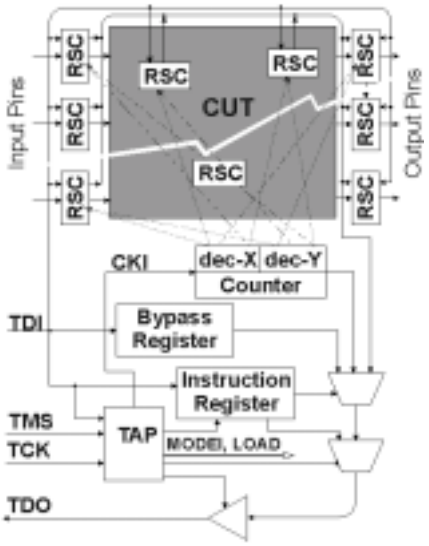

Fig. 2: Modified Random Access Scan – a general scheme

circuit is clocked with the functional clock CKI the cell works like a D-FF without any additional gates in the functional path. The TDI signal from the last cell of the input part of the BS is converted into the TDS and TDR signals with the help of the circuit from Fig. 3.

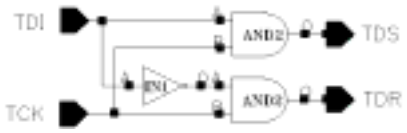

Fig. 3: Set / Reset decoder

The design of the internal RAS cell is given in Fig. 4. The 3-state buffer IT1 is controlled by the REI signal, which is connected with the REO output from the previous RAS cell. One TDO output of the RAS cell is activated within one clock cycle and its logical value comes from the cell with next address than is the current address. The TAP controller has the same functions as the BS standard TAP controller and it is completed with an address counter, address decoder and the circuitry for initializing the auxiliary D-FF and resetting the address counter.

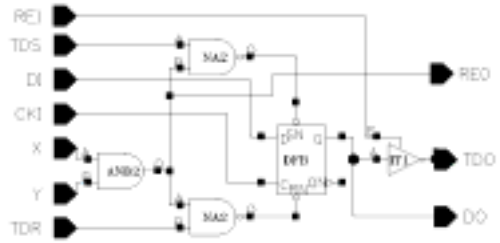

Fig. 4: Proposed internal RAS scan cell

When the TAP controller is in the ShiftDR state it causes that the address counter is clocked simultaneously with TCK. Shifting patterns and reading the CUT responses is performed in the same order as it is done in the BS design. The entire Master latches of the BS cells are loaded with the previous D-FF output value with the rising edge of the CKI. Simultaneously the addressed RAS cell is set or reset according to the value of TDS/TDR signals, the auxiliary D-FF is loaded with the actual logical value of the RAS cell, which has enabled the output; the address counter is clocked.

With the falling edge of the CKI signal the Slave latches in the BS cells are updated, the counter outputs are set to new values, the address decoders decode the new RAS cell address. In Fig. 2 we can see a general scheme of the circuit with RAS without any BS cells. It has the BS cells replaced with the I/O RAS cells from Fig. 5. This diagnostics access method works like the combined BS/RAS circuit, it has bigger hardware overhead and lower power dissipation because the BS cells are replaced with RAS cells with smaller power dissipation during test. The routability of the circuits with the RAS diagnostic access is the same as the routability of other methods (the ratio between the area of the cells and the area of the routing channels is the same for circuits with RAS and with a scan chain).

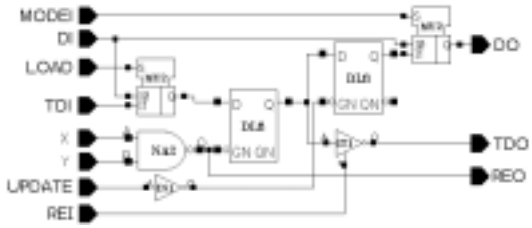

Fig. 5: Proposed I/O RAS scan cell (RSC)

IV. DESIGN OF MODIFIED BOUNDARY SCAN (RINGRAS)

In this design, we proposed a solution of the scan chain with substantially reduced impact on the CUT during shifting patterns and without any additional gate in the functional path. The main idea of this solution is described in [10] (Fig. 6).

The diagnostic access scheme consists of internal cells (Fig. 7) and two alternative types of I/O cells (Fig. 8 and Fig. 9). The I/O cells can be used instead of the BS cells in the BS design and the internal cells replace the scan chain cells from the BS design. The scheme is completed with an auxiliary feedback flip-flop chain. After activating the signal RES, the auxiliary flip-flop chain is set to a

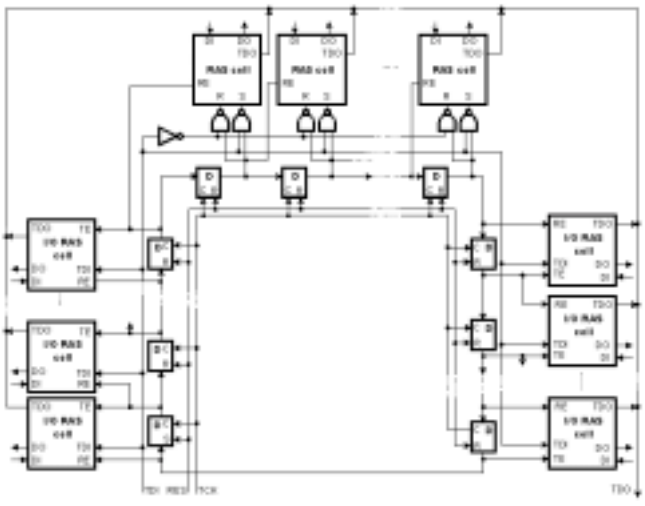
Fig. 6: Proposed MBS diagnostic scheme

state with only one logical one (the first bit) and all the other flip-flops are set to zero. During pattern loading the logical one is cyclically shifted through the auxiliary chain. The flip-flop with logical one enables test bit loading through the input TDI to the corresponding cell. Simultaneously it enables reading the state of the next cell to the output TDO. In the I/O cells the signal TDI is connected with the TDI input. In the internal cells, the TDI signal is used for feeding the input S. The inverted TDI signal is used for feeding the input R. These inputs asynchronously set and reset the cell flip-flops. In the diagnostic mode, the auxiliary chain flip-flops in the scheme are clocked with the signal TCK.

If the circuit is in the functional mode, the internal cells work like D-FFs without any additional

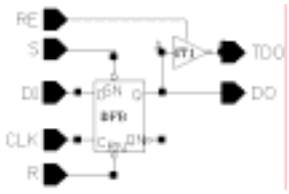

Fig. 7: Internal cell (ringRAS)

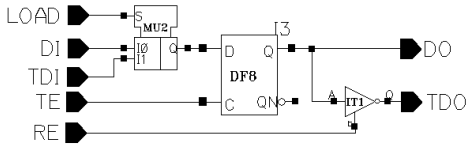

Fig. 8: Reduced I/O cell (ringRAS)

gates in the functional path. A single latch can substitute this FF according with the IC designer requirements.

We have designed all the circuits in the AMS 0.6 μm technology, and in this technology, there is not any latch with Set and Reset available, we have used D-FFs with Set and Reset asynchronous inputs instead of simple latches in the cells. The tri-state buffer IT1 (both in I/O and internal cells) is controlled by the RE signal, which is connected with the output of the neighbor auxiliary chain flip-flop output. The internal flip-flop has a Set and Reset asynchronous inputs. These inputs are controlled from the R and S cell inputs. The TAP controller has the same functions as the BS standard TAP controller.

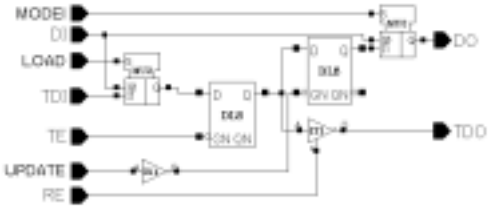

Fig. 9: I/O cell compatible with BS (ringRAS)

It is possible to use the proposed modified BS design combined with the standard BS design. In this case, we use BS cells on the inputs and outputs of the integrated circuit and the internal scan chain is replaced with the part of the proposed scheme corresponding to the internal RAS cells only.

V. DESIGN OF SYNCHRONOUS RANDOM ACCESS SCAN

The main idea of the proposed solution is described in Fig. 2. The functionality of the TAP controller and the compatibility with Boundary Scan standard (IEEE) is the same as in the previous chapters (II, III). Our proposed internal RAS cells (Fig. 10) replace all the internal flip-flops. During shifting the patterns through the scan chain, the RAS cells are activated according their addresses. The bits from the BS scan chain are loaded into the RAS cells. The actual values of unchanged RAS cells are kept with a help of a local feedback from Q output of I0 cell to I0 input of I2 multiplexer.

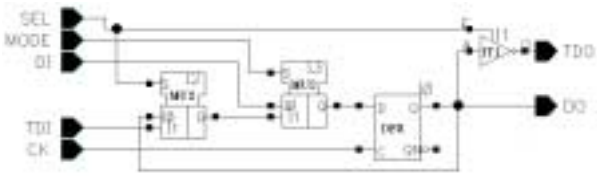

Fig. 10 – Internal sRAS cell

As it was formerly said, the main disadvantage of the RAS method is that it requires higher number of long connecting wires from address decoder to the relevant cells. We have designed the benchmark circuits both with one-wire and two-wire address decoder in order to demonstrate the influence of the number of the address wires to the hardware overhead.

VI. RESULTS

In Fig. 11, we show the hardware area of different benchmark circuits [4]. On the horizontal axis there are different circuits; on the vertical axis, the whole chip areas in square millimeters are given. All the designs were done with the Silicon Ensemble using AMS technology file (0.6 µm CUP-v3.30 [1]). We have designed eight circuits with different diagnostics accesses; the circuit areas do not include any boundary input and output cells and any TAP controller.

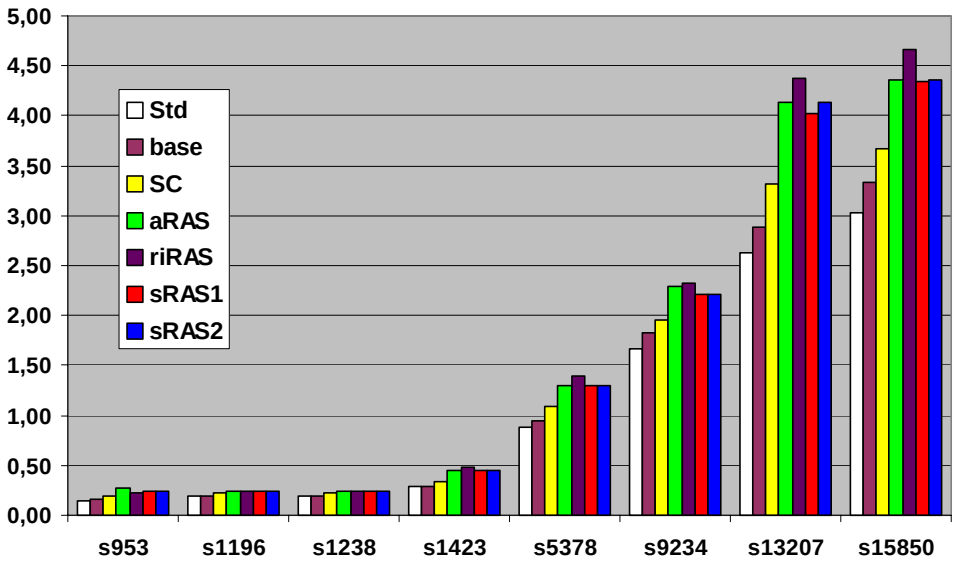

Fig. 11: Hardware overhead

For each circuit there are seven columns, which represent chip area for different diagnostics access methods. The first column “Std” represents the calculated standard cells area. Next column “base” presents the chip area of the basic benchmark circuit after floorplaning (routing the connections among the cells).

All the followed columns include additional cells, which are used for relevant diagnostics access. The third column “SC” shows the chip area of the Scan Chain presented in Chapter II, which is used in Boundary Scan design or in the standard Scan-design. The fourth column “aRAS” demonstrates the area of asynchronous RAS cells discussed in chapter III. We can see that the additional area (overhead) is rather big – about 30% comparing the area of the base chip. Nevertheless, it is necessary to say that the switching activity is lower [10]. The fifth column “riRAS” represents the modified Scan Chain, whose cells are activated by additional ring chain (see chapter IV). The last two columns show the hardware area of the synchronous RAS cells; columns named „sRAS1“ present one-wire-addressing scheme and „sRAS2“ present two-wire address. We can see that the increasing number of address wires does not cause lower hardware overhead.

The Random Access Scan has a big advantage of consuming lower amount of energy. We have designed a several kind of RAS cells, which can be used instead or together with the Boundary Scan cells and it has the same capabilities. The modification consists in adding an address counter and decoder. Our proposed RAS method has negligible power consumption during test in comparison with the serial scan chain methods. There is no need to reduce the clock speed during test or to energize the power source because of testing. On the contrary to the scan chain design, the proposed method does not add any delay into the functional path of the CUT.

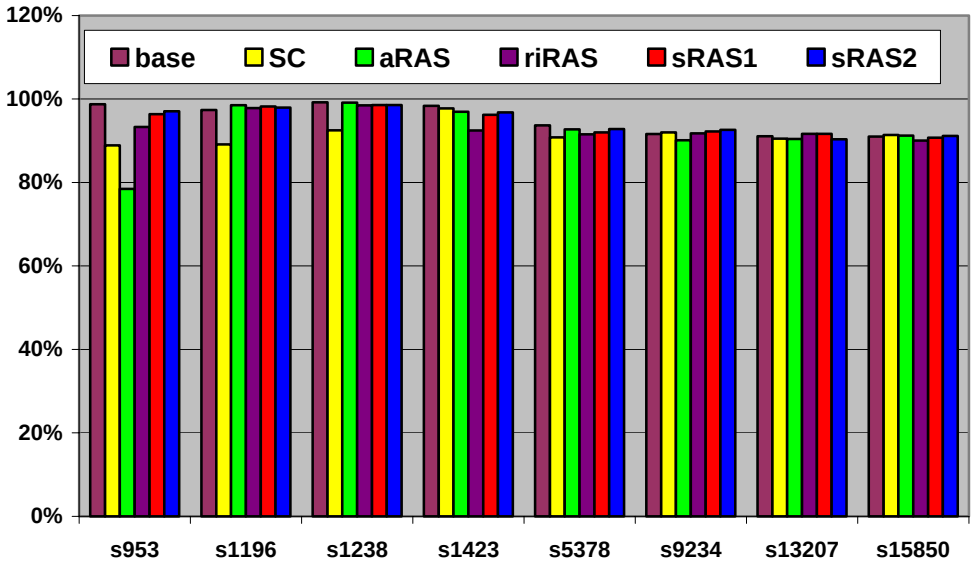

Fig. 12: Row Utilization Factor

The routability (ratio between standard cell area and area of the chip) of the benchmark circuits with different diagnostics access is presented in Fig. 12. The routability of our proposed RAS design is comparable to the routability of the base circuit description in the used technology. Hardware overhead of the RAS diagnostic circuitry is evidently greater than that for scan chain design (the number of the cells is higher). For many circuits this greater hardware overhead could be acceptable because of the benefit obtained from RAS advantages.

ACKNOWLEDGMENTS

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