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SCAN BASED CIRCUITS WITH LOW POWER CONSUMPTION

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Abstract: *In this paper we present a low power scan design method. Nowadays the Boundary Scan (BS) diagnostic access to the circuit input and output cells combined with a scan chain of concatenated internal flip-flops (FF) has become to be a standard. An alternative parallel diagnostic access method called Random Access Scan (RAS) is not used in nowadays ICs because of more difficult routability. In spite of this fact the diagnostic methods with a random access to IC FFs are much less energy consuming than any of the serial diagnostic approaches. They have a disadvantage of higher hardware overhead. In order to maximize power savings and minimize the hardware overhead we have proposed a modified RAS diagnostic access method, which can be used together with the BS. The RAS cells, controlled by the BS TAP controller, replace internal scan chain FFs, which are known as sources of unwanted circuit activity during shifting test patterns. We have calculated the hardware overhead of the RAS circuits and the power dissipated during loading test patterns. We have found that the proposed BS and RAS combination could be very useful for low power design and it does not introduce any additional delay in the functional path.*

1 Introduction

There are several methods how to move test patterns into the Circuit under Test (CUT). By the term CUT we mean a circuit or a module of a complex circuit, which has to be tested. If we speak about sequential circuits equipped with some of the diagnostic circuitry, CUT usually means the combinational part of the circuit only. As it is not usually possible to use the primary circuit inputs for test pattern insertion and the test patterns for complex circuits are generated in such a way that some diagnostic access to flop-flops (FF) is demanded, several diagnostic access methodologies were created. Usually a multiplexor is inserted to the original data input. One of the inputs is reserved for the functional data and the second functional input of this multiplexor is used as a diagnostic input data. The function is controlled by a mode signal. The diagnostic methodologies can be divided into serial access methods and random access methods. Historically the main representative of the serial diagnostic access methods was the method called LSSD [4] and the method Random Access Scan (RAS) [1] can serve us as a representative of the parallel methods. In 1993 a new serial method called Boundary Scan (BS) [2], [11] was standardized. This method enables scanning in and out circuit inputs and outputs and it can perform several other functions. During the last decade the serial diagnostic access methods became to be

the most important ones within all the diagnostic access methods and nowadays they are widely used. In order to further simplify testing of sequential circuits the BS is completed with a chain of scan cells (SC), which replace internal FFs. On the contrary to the chain of BS cells, the internal FF chain affects the CUT during shifting test patterns (Fig.1).

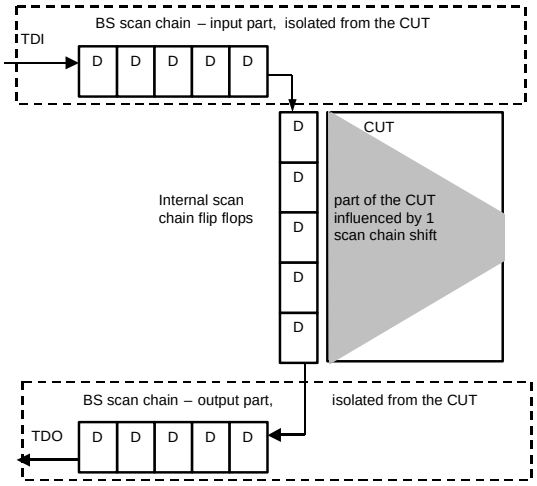

Fig. 1 BS circuit activity during shifting patterns

With growing size of the produced ICs new problems occurred: shifting test patterns in long scan chains causes unacceptably big heat dissipation, the test clock frequency has to be lowered and/or special gates avoiding signal wide spreading has to be used. This high consumption should be a problem in the novel battery powered portable devices and in the high clock frequency designs.

The RAS diagnostic access method is advantageous because it spares energy, which is necessary for reading and writing diagnostic data and it has no multiplexor on internal RAS FF input. The main disadvantage of the RAS method is that it requires higher number of wires and thus the hardware overhead is greater than it is in case of the BS.

Modern IC production technologies allow higher connectivity of the construction blocks of ICs and it seems that it could be possible to accept higher hardware overhead in order to get the advantages of random access diagnostic methods. The main advantage of the serial diagnostic access methods is that they need fewer wires for controlling the diagnostic data shifting through the scan chain. Another situation occurs if we want to have a diagnostic access to internal FFs. These internal FFs can be included into the scan cells (SC) but as the FF outputs are directly connected with the rest of functional logic shifting patterns through the scan chain causes an activity of the combinational part of the circuit (Fig. 1). An overview of methods for power minimization during testing is given in [7]. It is possible to reduce both average and peak power dissipation by generating test patterns in ATPGs, which minimize the number of transitions in the CUT between two consecutive vectors [16], [17], by reordering test patterns [8] or by modifying the order of scan FFs in the chain [5] and partitioning the scan chain [18], [13]. Experimental results on benchmark circuits show that a reduction ranging from 10% to 86% can be obtained by the mentioned techniques without fault coverage reduction. Excessive power dissipation is obtained in case of using built-in pseudo random pattern generator. It was shown that it is advantageous to filter patterns that do not detect faults [12]. By filtering we could get the power savings from 18 % to 78 %.

Another solution of the circuit activity reduction was proposed in [6] and [9]. These methods are based on the FF outputs gating with the help of a NOR gate. These solutions are effective from the power saving point of view but gating the FF outputs causes an additional delay in the critical functional path of the circuit. It is clear that the methods can be combined with other already mentioned solutions.

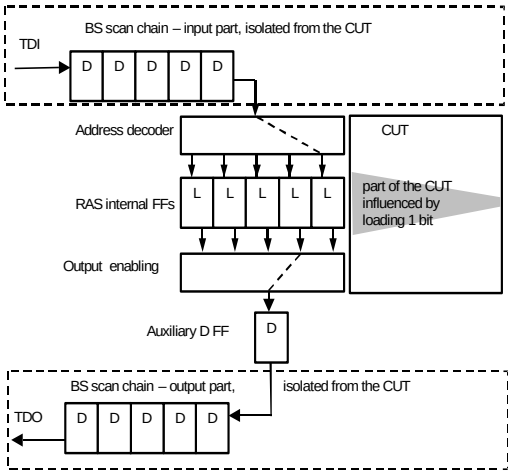

Fig. 2 Proposed BS/RAS diagnostic scheme

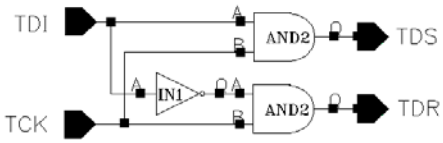

Fig. 3 Set / Reset decoder

Using the RAS diagnostic access methodology may be an alternative solution of the power minimization problem. In [14] and [15] a method of implementing RAS cells into a serial diagnostic access design was introduced. We have improved this solution and we offer full compatibility with Boundary Scan. We have exactly enumerated the hardware overhead devoted to the diagnostic equipment and we have done a comparison of the energy consumption for feeding test patterns into the Boundary Scan circuit and a proposed modified RAS circuit.

2 Design of Modified Random Access Scan

The main idea of the proposed solution is described in Fig. 2. After the reset the address is decoded in such a way that the output of the input part of BS is connected with the first RAS cell. The address signal is used also for read enabling of the cell with the consequent address. During shifting patterns through the scan chain the RAS cells are activated according their addresses and the bits from the BS scan chain are loaded into the RAS latches. The actual values of unchanged RAS cells are captured simultaneously with loading test patterns into cells in the auxiliary D-FF and then loaded into the output part of the BS chain. The output of the auxiliary D-FF of the first block feeds the diagnostic data inputs of the second part and so on. All the blocks have one common address counter, address decoder and addressing wires. This arrangement saves a substantial part of hardware overhead but it multiplies the power consumption.

We have designed all the circuits in SiliconEnsemble (0.6 μm technology (AMS-cub) [10]. In this technology there is not any latch with Set and Reset inputs available, we have used D-FFs with asynchronous Set and Reset inputs instead of simple latches. If the circuit is clocked with the functional clock CKI the cell works like a D-FF without any additional gates in the functional path. The TDI signal from the last cell of the input part of the BS is converted into the TDS and TDR signals with the help of the circuit from Fig. 3.

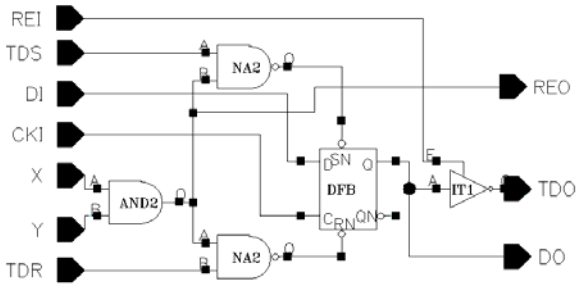

Fig. 4 Proposed internal RAS scan cell

The design of the internal RAS cell is given in Fig.4. The 3-state buffer IT1 is controlled by the REI signal, which is connected with the REO output from the previous RAS cell. One TDO output of the RAS cell is activated within one clock cycle and its logical value comes from the cell with next address than is the current address.

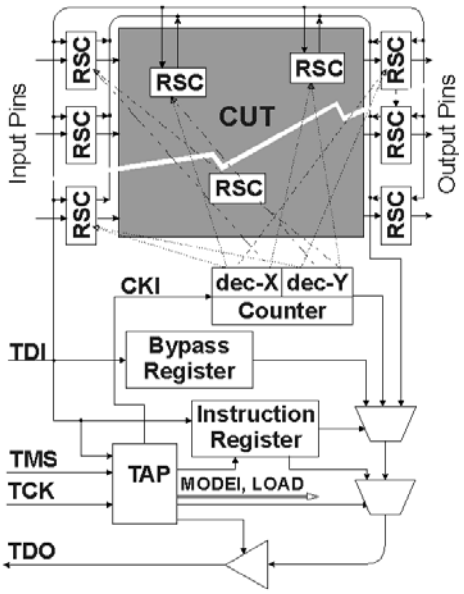

Fig. 5 Modified Random Access Scan – a general scheme

The TAP controller has the same functions as the BS standard TAP controller and it is completed with an address counter, address decoder and the circuitry for initializing the auxiliary D-FF and resetting the address counter.

When the TAP controller is in the Shift state [2] it causes that the address counter is clocked simultaneously with TCK. Shifting patterns and reading the CUT responses is performed in the same order as it is done in the BS design. The entire Master latches of the BS cells are loaded with the previous D-FF output value with the rising edge of the CKI. Simultaneously the addressed RAS cell is set or reset according to the value of TDS/TDR signals, the auxiliary D-FF is loaded with the actual logical value of the RAS cell, which has enabled the output; the address counter is clocked.

With the falling edge of the CKI signal the Slave latches in the BS cells are updated, the counter outputs are set to new values, the address decoders decode the new RAS cell address. In Fig. 5 we can see a general scheme of the circuit with RAS without any BS cells. It has the BS cells replaced with the I/O RAS cells from Fig. 6. This diagnostics access method works like the combined BS/RAS circuit, it has bigger hardware overhead and lower power dissipation because the BS cells with bigger power dissipation are replaced with RAS cells with smaller power dissipation during test. A set of benchmark circuits from [3] was used for comparison of the chip area, both with a scan chain and with modified RAS cells. A comparison of the hardware overhead of these circuits is given in Fig. 7. The routability of the circuits with the RAS diagnostic access is the same as the routability of other methods (the ratio between the area of the cells and the area of the routing channels is the same for circuits with RAS and with a scan chain).

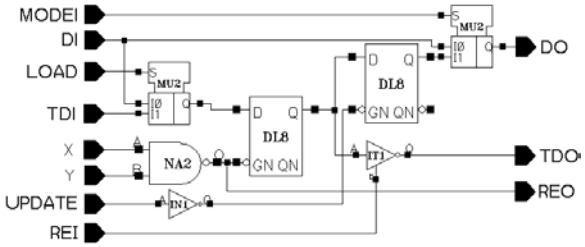

Fig. 6 Proposed I/O RAS scan cell (RSC)

3 Power consumption of BS and RAS circuits

Power dissipation in digital CMOS circuits is divided into static and dynamic one. The static power is comparing to the dynamic one negligible. The average dynamic power of synchronous digital circuits is proportional to the total node transition count (NTC) divided by the number of clock cycles [13]. In [13] a formula deriving the NTC is derived:

$$NTC = \sum_{i \in G} N_{Gi} C_{Gi} + \sum_{i \in FF} (Low_{FFi} + High_{FFi})$$

where N_{Gi} is the total number of gate output transitions (from 0 to 1 and vice versa) for the i-th gate and C_{Gi} is its load capacitance. The load capacitance for each combinational circuit is equal to the number of fan-outs. The sum is done over all combinational gates.

	NTC of the comb. part of the CUT		
	SC	**RAS**	**ratio%**
s641	116	2,2	1,9
s713	121	2,2	1,9
s953	111	2,5	2,2
s1196	81	2,5	3,1
s1238	81	2,5	3,1
s1423	313	3,4	1,1
s5378	1258	5,9	0,5
s9234	2560	10,4	0,4
s13207	4105	5,9	0,1
s15850	4050	6,6	0,2

Tab. 2 NTC of combinational parts of the circuits during shifting random patterns through the internal FFs.

No. of FFs	SC		RAS	
	1,024 bits	2,048 bits	1,024 bits	2,048 bits
clk tree	2097,15	8388,61	20,480	40,960
SC/RAS cells	4194,30	16777,22	4,096	16,384
Addr. decoder			8,192	32,736
Addr. counter			8,184	16,368
TDS, TDR			524,288	2097,152
Total NTC	6291,45	25165,82	565,240	2203,600

Tab. 1 Comparison of SC and RAS NTC caused by shifting 1024 and 2048 random bites through the SC and RAS circuits.

Low_{FFi} is the minimal NTC of the i-th FF. For MS FFs $Low_{FFi} = 2*\mathrm{Clk_L}$, where Clk_L is the number of clock cycles for which the FF input has the same value as the FF output.

$High_{FFi}$ is the maximal NTC of the i-th FF. For MS FFs $High_{FFi} = 6*Clk_H$, where Clk_H is the number of clock cycles for which the FF input has different value from the FF output.

Let us assume that we have a circuit with 1024 FFs or 2048 FFs concatenated into a scan chain and a RAS circuit with the same number of RAS cells. We have calculated the average energy consumed in diagnostic circuitry during loading a test pattern. The NTCs of the RAS and SC diagnostic equipment are given in Tab. 1. We can see that the RAS diagnostic equipment is consuming less then 10% energy of the energy consumed by the scan-chain In Tab. 2 we give the medium values of the NTC obtained during shifting patterns through circuits with SC or modified RAS diagnostic access. The average values of NTCs are obtained as a ratio between the total NTC and number of performed clock cycles. We can see that the activity of the CUT with RAS is substantially lower than for BS. Comparing with the power reduction techniques described in [6] and [13] the proposed method has lower average power consumption. The proposed solution of the BS/RAS diagnostic access has lower average power dissipation during test than is the normal circuit function power dissipation.

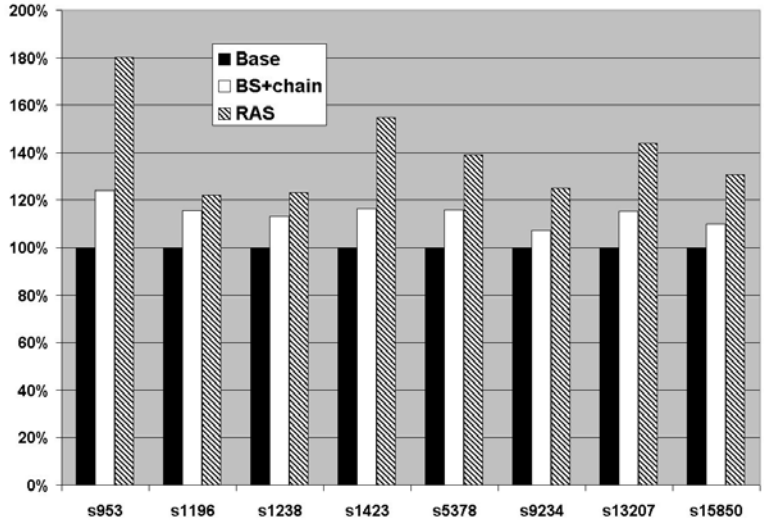

Fig. 7 Hardware overhead (AMS 0.6μm technology) of ISCAS circuits using standard scan chain cells compared with circuits using modified RAS cells.

4 Conclusion

The Random Access Scan has an advantage of consuming lower amount of energy comparing with a scan chain design. It cannot be used simultaneously with the Boundary Scan because of more complex controlling and different timing. We have designed

a new RAS diagnostic access method, which can be used instead or together with the Boundary Scan method and it has the same capabilities. The modification consists in adding an address counter and an auxiliary FF that synchronises the addressed RAS cell output with the BS chain input. We can resume the advantages and a disadvantage of the proposed method:

- Proposed RAS method has negligible power consumption during test in comparison with the scan chain methods. There is no need to reduce the clock speed during test or to energize the power source because of testing.
- On the contrary to the scan chain design the proposed method does not add any delay into the functional path of the CUT.
- Hardware overhead of the diagnostic circuitry is greater than that for scan chain design (the number of the cells is higher) but the global routability is the same.

For many circuits the greater hardware overhead could be acceptable because of the benefit obtained from RAS advantages. It is possible to concatenate several blocks of RAS cells and to use only one address counter and decoder; the hardware overhead of such solution is relatively low. The number of concatenated blocks can be chosen as a trade off between energy savings and hardware overhead. Using more blocks of RAS cells makes possible to use low power diagnostic access even for large circuits with great number of internal FFs.

Acknowledgments

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