PLIVA, Z., NOVAK, O., BOURDEU d'AGUERRE, P. : Hardware Overhead of Boundary Scan and RAS Design Methodologies, Proc. of DDECS2002, April 17-19, 2002, Brno, pp. 36-43, ISBN 80-214-2094-4

HARDWARE OVERHEAD OF BOUNDARY SCAN AND RAS DESIGN METHODOLOGIES

Zdeněk Plíva, Ondřej Novák
Technical University of Liberec
Hálkova str. 6, CZ-46117 Liberec
zdenek.pliva|ondrej.novak@vslib.cz

Philippe Bourdeu d'Aguerre
Campus de l'INSA
Rangueil, 31077 Toulouse Cedex 4 - France
bda@aime.insa-tlse.fr

Abstract. *In this paper we present results of our experiments with integrated circuit BISTE (Built-In Self Test Equipment) design. We have designed several kinds of BISTE in nowadays technologies and we have found that the hardware overhead could be significantly lowered when using appropriated BISTE technique. Nowadays the Boundary Scan (BS) diagnostic access to the circuit input and output cells has become to be a standard and the alternative parallel diagnostic access called Random Access Scan (RAS) has been abandoned by the designers. In spite of this fact diagnostics with the random access to IC boundary is much less energy consuming than any of the serial approaches. We have compared the hardware overhead of the BS diagnostic equipment with the RAS design and we have found that the second one can be built on lower IC area. We have built the RAS diagnostic equipment in such a way that it has the same controlling circuitry as BS and it could be used alternatively. Further area reduction can be obtained by using built-in test pattern generators on chip. These generators spare the memory, which is necessary for storing the test vectors. The pattern generators can be got by simple modification of the on-chip diagnostic equipment and thus we have adapted the BS cells to be used as a test pattern generator. We have found that when using this kind of test pattern generators the total area devoted for diagnostics is the lowest within the above-described approaches.*

1 Introduction

During the last decade serial diagnostic access methods became the most important within all diagnostic methodologies and they are widely used. These diagnostic access methods were standardised and the IEEE 1149 standard [3][10] called Boundary Scan (BS) is used for designing complex circuits. With growing size of produced integrated circuits new problems occurred: Shifting test patterns in long scan chains causes unacceptably big heat dissipation, the test clock frequency has to be lowered and/or special gates avoiding signal wide spreading has to be used. As modern IC production technologies allow higher connectivity of the construction blocks of ICs the following question arises: Is it necessary to use serial diagnostic access methods or could it be possible to use some parallel method? Historically the Random Access Scan (RAS) was considered to be an alternative to the serial methods. It has several advantages:

- it uses simpler construction blocks,
- it allows to read a logical value from a wire without any flip-flop
- it spares energy which is necessary for reading and writing diagnostic data.

The main disadvantage of the RAS method is that it requires higher number of long connecting wires.

In this paper we demonstrate our design of RAS like diagnostic cells, which have the same controlling signals as they are used in BS diagnostic cells. We compare the ISCAS circuits

designed with the help of proposed RAS cells with the same circuits designed with the BS diagnostic cells. As it is possible to further reduce the hardware overhead by using a built-in test pattern generators (TPG) [9] we propose a design of modified BS scan chain, which can be used as a TPG. The hardware overhead of the ISCAS circuits containing the TPG and a memory for storing the TPG seeds is compared with the overhead of the circuit with non-modified BS and corresponding memory for storing test patterns. In this paper we use as a TPG an automaton based on the cellular automaton with the rule 60 as it was shown in [6][14] and we have adopted the BS environment for converting it to the CA. We compared the total overhead devoted to the testing for the TPG based and classical test-per-scan approach with compacted deterministic test patterns.

2 Test pattern insertion methods

There are several methods how to move test patterns into the Circuit Under Test (CUT). As it is not usually possible to use the primary circuit inputs for test pattern insertion and the test patterns for complex circuits are generated in such a way that a diagnostic access to flip-flops is demanded, several diagnostic CUT access methodologies were created. Usually a multiplexor is inserted to the original data input. The second functional input of this multiplexor is connected with the diagnostic input signal and the multiplexor function is controlled by a mode signal. The diagnostic access methodologies [15] can be divided into serial access methods and random access methods. Historically the main representative of the serial diagnostic access methods was the method called LSSD [7] and the method Random Access Scan (RAS) [2] could serve us as a representative of the parallel methods. Both of the mentioned methods were proposed for scanning in and out the internal flip-flop bits only. In 1993 a new serial method called Boundary Scan (BS) was standardized. This method was designed so that it enables scanning in and out circuit inputs and outputs and it can be used for performing several other functions. The BS IC equipment is shown in Fig 1. Data flow is managed by TAP (Test Access Port) controller which is driven by TMS (Test Mode Select) and TCK (Test Clock). TAP controller can set each of the BSCs (Boundary Scan Cell) to the normal function – data coming from Input Pins are connected to the inputs of the CUT. In Scan mode it is possible to send serial input data from TDI (Test Data Input) through the shift register to the relevant BSC. In reverse it is possible to export serially all the BSC's outputs to TDO (Test Data Output). TAP controller can also bypass the IC using the Bypass Register.

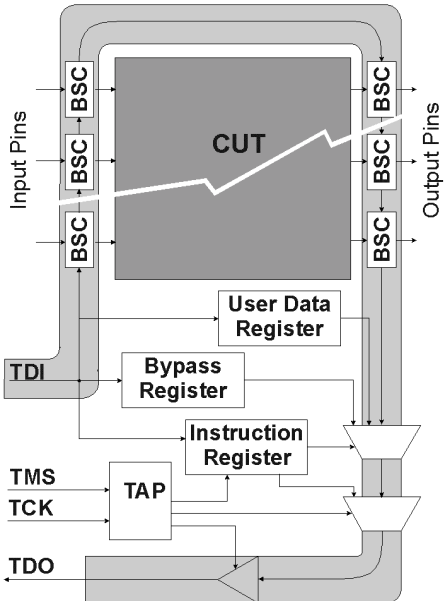

Fig 1: Boundary Scan – the principle scheme

The main advantage of the serial diagnostic access methods is that they need fewer wires for controlling the diagnostic data shifting through the scan chain. A main disadvantage of this approach is that it needs two D flip-flops for every controlling and observing IC point. Another disadvantage of the serial methods is that big switching activity in test mode causes an inappropriate growth of the power consumption. This high consumption should be a problem in the novel battery powered portable devices and in the high clock frequency designs.

In the RAS method each observing and controlling point has a unique address. The addresses are decoded usually in two decoders (column and row decoders). This arrangement causes that the area overhead of the wires on the IC is higher but the flip-flops can be simpler and in some cases they can be omitted. In the past, the disadvantages of RAS were found to be more important than the advantages and the serial methods are preferred.
The nowadays IC production technologies have dramatically better connectivity of functional blocks and it is an open question whether it will not be more useful to use random access methods instead of the serial ones.

3 Design of Modified Random Access Scan

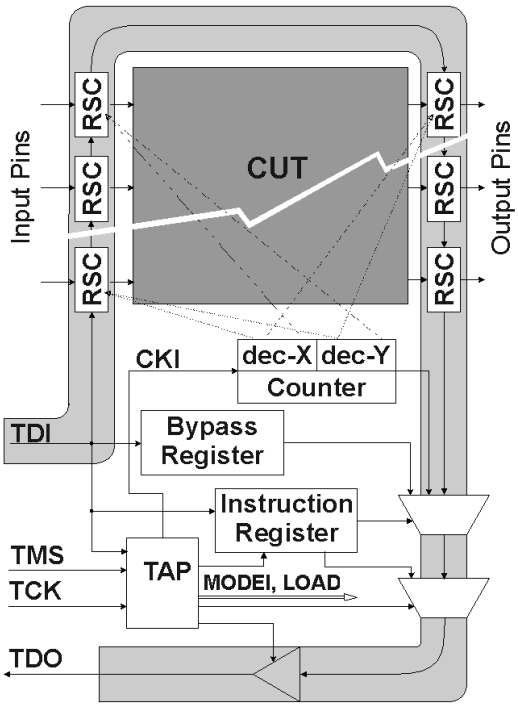

Fig 2: Random Access Scan – a general scheme

In Fig 2 we can see a general scheme of the modified RAS method. This diagnostic access method uses a TAP controller, which is similar to the TAP controller from the BS and which is completed with a counter and address decoders. This counter can be designed instead of the user defined register from the original TAP controller. We designed a RAS cell (see Fig 3), which replaces original BS cells. The RAS cells are connected with the TAP controller with the help of X signals, Y signals and MODEI and LOAD signals. The X and Y signals are activated from dec-x and dec-y decoders. It could be possible to use one address decoder only, but the proposed solution with two decoders forming the two wire address signals was less hardware consuming. Tri-state buffers IT1 are controlled by the address X and Y signals and they activate the output TDO. If activated the TDO output has a logical value coming from the addressed RAS cell.

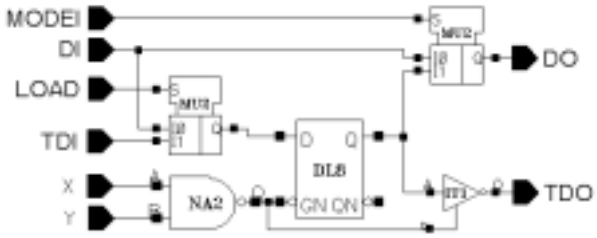

Fig 3: Proposed modified RAS cell

A comparison of the hardware overhead of the Boundary Scan and our proposed modified RAS is given in Tab. 2. In both of the used methods we need similar TAP (Test Access Port) controllers for generating all the control signals.

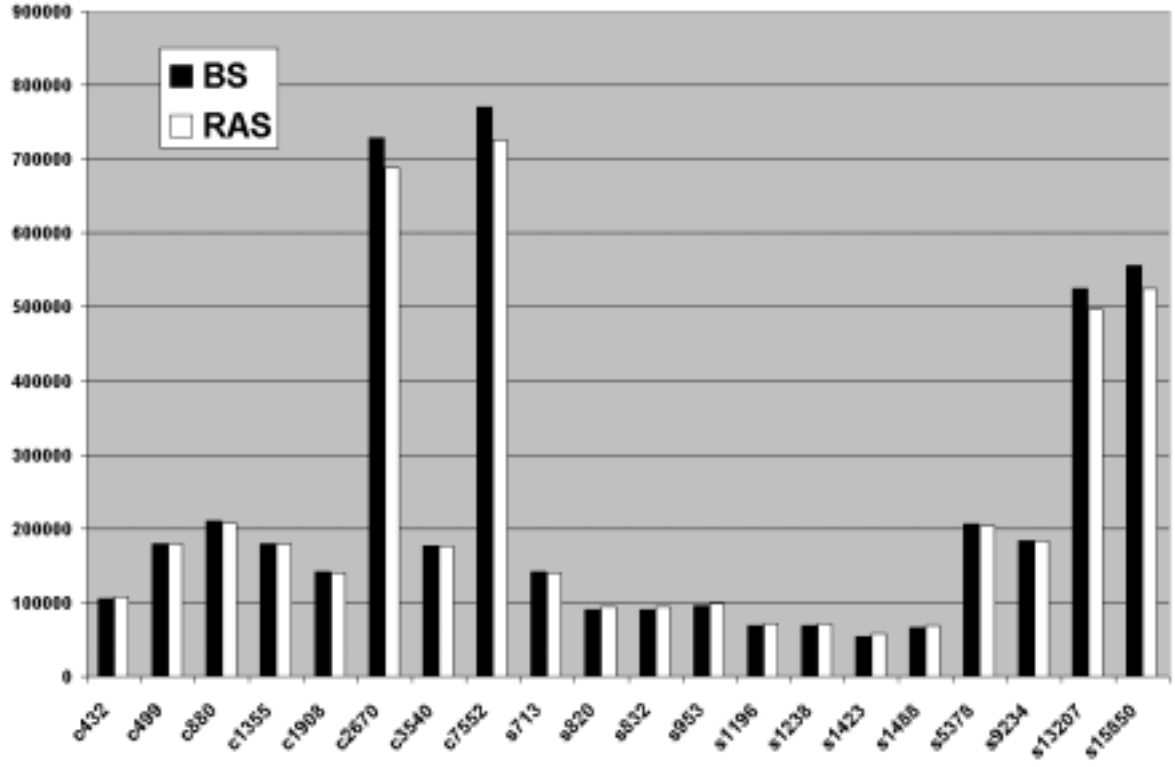

Fig 4: Hardware overhead of the BIST using standard BS compared with the BIST using modified RAS [um^2] (also Tab. 2).

The hardware overhead of these controllers is not included in the table. In Fig 4 we can see a graph of the hardware overhead comparison from Tab. 2. The overhead of the modified RAS is rarely larger than the overhead of BS. We can see that for large circuits the modified RAS diagnostic method is less hardware consuming but for some of smaller circuits it is not true. One example of a circuit for which the BS overhead is smaller is the circuit S953. This situation is caused by higher area consumption, which is necessary for building counter and decoders then is the saving which is obtained by using simpler cells.
The average power consumption of synchronous digital circuits is proportional to the total node transition count

	NTC of the combinational part of the CUT		
circuit	**BS**	**RAS**	**ratio %**
s641	116	2,2	1,9
s713	121	2,2	1,9
s953	111	2,5	2,2
s1196	81	2,5	3,1
s1238	81	2,5	3,1
s1423	313	3,4	1,1
s5378	1258	5,9	0,5
s9234	2560	10,4	0,4
s13207	4105	5,9	0,1
s15850	4050	6,6	0,2

Tab. 1: Average circuit activity

(NTC) divided by the number of clock cycles [11]. In Tab. 1. we can see the estimated switching activity of selected benchmark circuits during test. We can see that the activity of the CUT with RAS is substantially lower than the activity for BS.

circuit	BS	RAS
c432	105419	107686
c499	178967	179087
c880	210838	207871
c1355	178967	179087
c1908	142193	140899
c2670	728128	688073
c3540	176516	176873
c7552	769805	725715
s713	142193	140899
s820	90709	94401
s832	90709	94401
s953	95613	98829
s1196	68645	71514
s1238	68645	71514
s1423	53935	58229
s1488	66193	69300
s5378	205935	203443
s9234	183871	183515
s13207	524644	496262
s15850	556515	525047

Tab. 2: Hardware overhead of the BIST using standard BS compared with the BIST using modified RAS [um^2].

circuit	BS	TBS
c432	204490	214972
c499	307773	306706
c880	309909	360151
c1355	328591	331140
c1908	291816	278735
c2670	934710	1002149
c3540	349180	329041
c7552	1108151	1224951
s713	254431	269738
s820	221257	119187
s832	221257	117613
s953	255339	130967
s1196	234641	98684
s1238	239179	103406
s1423	202294	186690
s1488	176622	158551
s5378	692231	325354
s9234	738967	385928
s13207	3070936	876838
s15850	1614363	935603

Tab. 3: Total hardware overhead of the BIST and memory for storing the test patterns using standard BS compared with the BIST using built-in TPG [um^2].

4 Built-in Test Pattern Generator

In [12] we studied different TPG structures – linear feedback shift register (LFSR) based on D flip-flops and XORs in the feedback, the cellular automata (CA) based on D flip-flops and XORs in the local feedback taps and the T flip-flop based CA. We found that the CA has a lot of advantages from several points of view. The test patterns generated in such a TPG have better random properties than for example patterns from the LFSR based TPG. The fault coverage of a limited number of generated patterns is higher then the fault coverage of the other automata test pattern sequences with the same length.

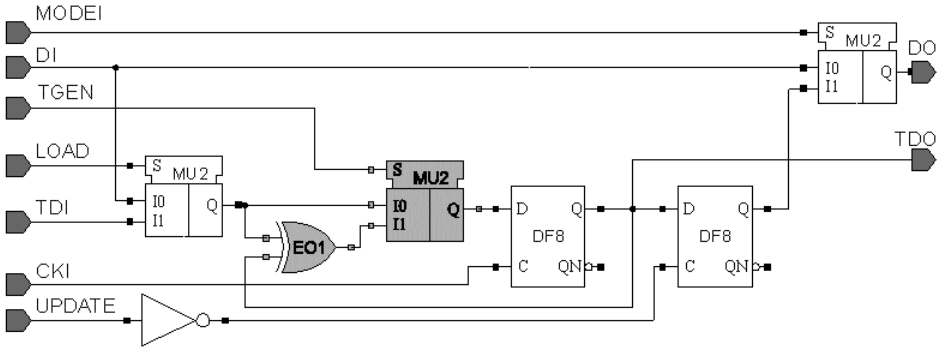

Fig 5: Modified BS Cell (TBSC)

In order to allow designers of the circuits with BIST to use standard software tools for the TPG insertion we have modified Boundary Scan Cell (BSC) into the TBSC cell . The cell is modified in the manner given in Fig 5. Newly added circuits are colored with the gray color. If the TGEN signal equals to 0 the TBSC cell has original BSC functionality. By changing TGEN to 1 we activate a local feedback that converts the D flip-flop into the T flip-flop. After connecting the TDO outputs of the cells with TDI inputs so that they are connected into a chain and after adding a global feedback tap from the last TDO to the first TDI we obtain a CA that can be used as a TPG.

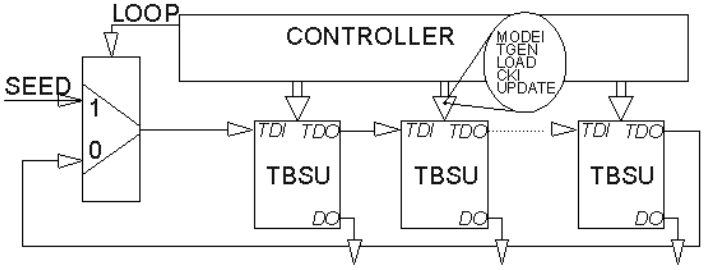

Fig 6: Resulting TPG

In Fig 6 we can see a simple scheme, which was designed for examining the functionality of a TPG consisting from TBSC cells and a multiplexor. We have simulated a TPG consisting of 17 TBSC cells with a global feedback. The feedback can be broken by the multiplexor with the help of the control signal LOOP. We are able to move new seed into the TPG through the scan chain by breaking the feedback and switching off TPG mode (TGEN signal) . After seeding the TPG generates a test sequence, which can be deflected with a help of the SEED input in such a way that the test patterns detecting hard-to-test faults are generated [12]. All the test patterns are shifted to the DO output of the TBSC by using the UPDATE signal in the test mode (MODEI = "1"). In next figure (Fig 7) we can see the time diagrams of this TGP, which were simulated in VerilogXL in order to verify the TPG functionality.

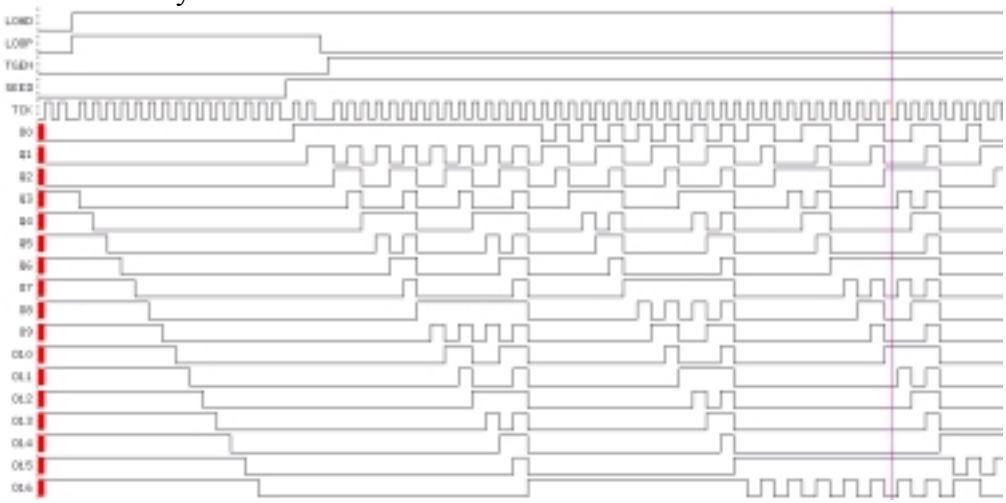

Fig 7: Time diagram of the simulation of the TPG functionality

At the beginning (see Fig 7) all the control signals was set to 0 and TDO outputs of the TPG equals to 1 (or the random state). By changing the LOOP and LOAD signals we set up all the TPG cells. After that the feedback is rebuild (LOOP=0), generating mode is activated (TGEN=1) and the following clock cycles causes the pattern generation.

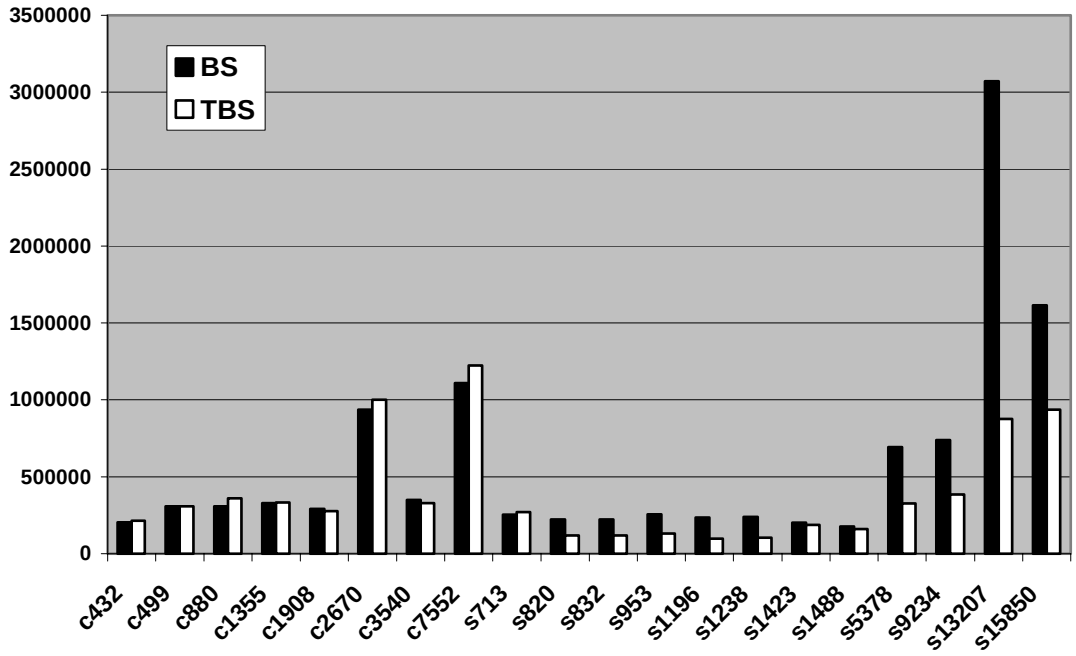

Fig 8: Hardware overhead of the BIST using standard BS and a memory for storing the test patterns compared with the BIST using built-in TPG [um^2] (also Tab. 3.).

We have re-designed the ISCAS benchmark circuits [4][5] in order to give them a possibility of built-in test pattern generation. We have chosen the circuits, which are hardly testable by a pseudoexhaustive test set. We have computed the input TPG sequence that has to be introduced into the TPG in order to complete the generated test sequence with patterns, which test the hard-to-test faults. The fault coverage of the generated test sequence was 100%. We have built a memory, which is necessary for storing the input TPG sequence. All the designing steps (Verilog netlisting, schematics, floorplaning) were done in IC-package by Cadence Design Systems. We have used the AMS **Chyba! Nenalezen zdroj odkazů.** technology files 0.6 micron (double-metal CMOS standard cells 5.0V). The memory structures were generated with the help of the AMS tool from the web pages **Chyba! Nenalezen zdroj odkazů.**. For some circuits we have built a ROM memory, for some other a RAM memory and for the smallest circuits we have stored the input TPG sequence in D flip-flop shift register. The choice was done in such a way that a minimal hardware overhead was obtained.

The names of the used benchmark circuits are in the first column of Tab. 3. The second column presents the total hardware overhead of the BIST containing a memory and the given circuit with Boundary Scan. The memory contains deterministic compacted test patterns [8]. The third column demonstrates the hardware overhead of our modified Boundary Scan (TBS) method with built-in TPG. The graphical comparison of this table is in Fig 8. Since the test patterns are generated in the TPG the memory stores only the TPG seed and (or) the modifying bits [13].

We can see that for large circuits the diagnostic method TBS is substantially less area consuming than any method of circuit testing with deterministic patterns and BS or RAS. This is not true for small circuits, which are better to be tested without any built-in TPG. In those cases the total accrual of the TBSCs is larger than the spared memory.

5 Conclusion

As the Random Access Scan has an advantage of consuming lower amount of energy comparing with Boundary Scan we have designed a new RAS diagnostic access method. This method can be used instead of the Boundary Scan method and it has the same capabilities. We can access not only the internal flip-flops but also inputs and outputs of the RAS circuit, which gives us an opportunity of testing wires between different circuits equipped with diagnostic access.
We have found that for large circuits the hardware overhead of the proposed RAS environment is lower than the overhead of the Boundary Scan environment.
In accordance with previously published results we know that the lowest cost (measured by the total IC area) of diagnostics can be obtained for those methods that integrate test pattern generators into the scan chains. We have designed a modified Boundary Scan cell, which can be used for construction of the TPG. We compared the total resulting IC area, which is necessary for testing with the area, which is necessary for classical diagnostic approach with Boundary Scan. For large circuits the solution of BISTE with built-in test pattern generator was more efficient than the other methods.

Acknowledgments

The research was in part supported by the IST-2000-30193 grant (REASON), by the research grants of the Czech Grant Agency GACR 102/01/0566 and of the Ministry of Education, Youth and Sport MSM 242200002.

References

[1] http://asic.amsint.com/

[2] Ando, H., “Testing VLSI with random access scan”, Diag. Papers Compcon 80, IEEE pub. 80CH1491-OC, pp. 50-52, Feb. 1980

[3] Bleeker, H. “Boundary-Scan Test, a practical approach”, ISBN 0-7923-9296-5, 1993.

[4] Brglez, F., Fujiwara, H., "A Neutral Netlist of 10 Combinational Benchmark Circuits," Proc. IEEE Int'l Symp. Circuits and Systems”, IEEE Press, Piscataway, N.J., 1985, pp. 695-698; (http://www.cbl.ncsu.edu/benchmarks).

[5] Brglez, F., Bryan, D., Kozminski, K., "Combinational Profiles of Sequential Circuits," Proc. IEEE International Symposium of Circuits and Systems (ISCAS'89), Portland, OR, May 1989.

[6] Chaudhuri, P.P. et al., “Additive Cellular Automata Theory and Applications” Volume I. IEEE Computer Society Press, 1997, 340 pp

[7] E.B. Eichelberger and T.W. Williams, "A Logic Design Structure for LSI Testability," J. Design Automation and Fault-Tolerant Computing”, vol. 2, 1978, pp. 165-178.

[8] Hamazaoglu, I. - Patel, J.H.: Test Set Compaction Algorithms for Combinational Circuits. Proc. of International Conf. on Computer-Aided Design, November 1998

[9] Hlavicka J., Novak, O., “Built-in Self-Test Equipment - State of the Art”, Proc. of DDECS'97, Ostrava

[10] IEEE Std 1149.1-1993, IEEE Standard Test Access Port and Boundary Scan Architecture.

[11] Nicolici, N., Al-Hashimi, B. M., "Scan Latch Partitioning into Multiple Scan Chains for Power Minimization in Full Scan Sequential Circuits", Proc. DATE-2001, March, 2001, Paris, France

[12] Novak O., Hajek D., Nosek J., “Optimised hardware test pattern generator for BIST”, Proc. DDECS 2000, pp. 205-208

[13] Novak, O., Hlawiczka, A., Garbolino, T., Guczwa, K., Pliva, Z., Nosek, J., “Low Hardware Overhead Deterministic Logic BIST with Zero-Aliasing Compactor”, Proc. IEEE DDECS conf. Györ (Hungary)

[14] Pliva, Z., Novak, O., Bourdeu d'Aguerre, P., „Hardware Overhead of BIST Equipment“, Proc. of AE2001, Sept 2001, Pilsen, pp. 204-207, ISBN 80-7082-758-0

[15] Williams T.W., Parker K.P., “Design for Testability-A Survey”, proc. IEEE vol.71, 1983, pp.98-112