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# LOW POWER BOUNDARY SCAN DESIGN

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## Abstract

**In this paper we propose a low power modification of scan design methodology. Nowadays the Boundary Scan (BS) diagnostic access to the circuit input and output cells combined with a scan chain of concatenated internal flip-flops has become to be a standard. In case of sequential circuits, unwanted transitions of the circuit nodes, which are present during shifting test patterns, cause unacceptable high power consumption. It is possible to use an alternative parallel diagnostic access method originally called Random Access Scan (RAS), which has substantially lower power consumption and which does not introduce unwanted node transitions during loading test patterns into the circuit. The main disadvantage of the RAS is that it uses a big amount of wires, which control the RAS cells. In order to maximize power savings and minimize the hardware overhead we have proposed a modified BS diagnostic access method, which combines RAS and BS diagnostic access. The method has a lower number of wires than the RAS, it does not cause unwanted node transitions in the circuit during test patterns loading and the modified cells have lower power consumption than it is in the case of BS. All the proposed modified BS cells are controlled by the normal BS TAP controller.**

## 1 Introduction

In this paper we discuss possibilities of reduction of the power used for loading test patterns into a Circuit Under Test (CUT). By the term CUT we mean circuit or a module of a complex circuit, which has to be tested in one test session. There are several methods how to move test patterns into the CUT. If we speak about sequential circuits equipped with some of the diagnostic access circuitry we usually mean by the term CUT the combinational part of the circuit only. As it is not usually possible to use the primary circuit inputs for test pattern insertion and the test patterns for complex circuits are generated in such a way that some diagnostic access to flip-flops (FF) is demanded, several diagnostic access methodologies were created. Usually a multiplexor is inserted to the original data input. One of the multiplexor inputs is reserved for the functional data and the second functional input is used as a diagnostic data input . The multiplexor function is controlled by a mode signal.

The diagnostic access approaches can be divided into serial access methods and random access methods. Historically the main representative of the serial diagnostic access methods was the method called LSSD [4] and the method Random Access Scan (RAS) [1] can serve us as a representative of the parallel methods. LSSD was proposed for scanning in and out the internal FF bits only. RAS could be used also for observing logical values on wires. In 1993 a new serial method called Boundary Scan (BS) was standardized [2], [7]. This method was designed so that it enables scanning in and out the circuit inputs and outputs and it can perform several other functions. During the last decade the serial diagnostic access methods became to be the most important ones within all the diagnostic access methods and nowadays they are widely used. In order to further simplify testing of sequential circuits the BS is completed with a chain of scan cells (SC), which replace internal FFs. On the contrary to the chain of BS cells the internal FF chain influences the CUT internal combinational logic during shifting test patterns. With growing size of the produced integrated circuits new problems occurred: Shifting test patterns in long scan chains causes unacceptably big heat dissipation, the test clock frequency has to be lowered and/or special gates avoiding signal wide spreading has to be used. This high consumption should be a problem in the novel battery powered portable devices and in the high clock frequency designs.

The RAS diagnostic access method spares energy which is necessary for reading and writing diagnostic data and it has no multiplexor on internal RAS FF input.

The main disadvantage of the RAS method is that it requires higher number of wires and thus the hardware overhead is greater than it is in case of the BS.

In this paper we propose an idea how to mix BS and RAS diagnostic access methods in order to obtain advantages of both. In Section 2 we describe main principles of the BS method and the methods how to reduce its power consumption. In Section 3 we give a principal scheme of the modified BS (MBS) method and a description of the MBS cells. In Section 4 we compare the power dissipation during test and the hardware overhead for BS and MBS.

## 2 Test pattern insertion methods

The main advantage of the serial diagnostic access methods is that they need fewer wires for controlling the diagnostic data shifting through the scan chain.

The BS IC equipment is shown in Fig. 1.The data flow is managed by a TAP (Test Access Port) controller, which is driven by TMS (Test Mode Select) and TCK (Test Clock) signals. In the scan mode it is possible to send serial input data from TDI (Test Data Input) through the shift register to the relevant Boundary Scan Cell (BSC). Simultaneously it is possible to export serially all the BSC outputs to the output TDO (Test Data Output).

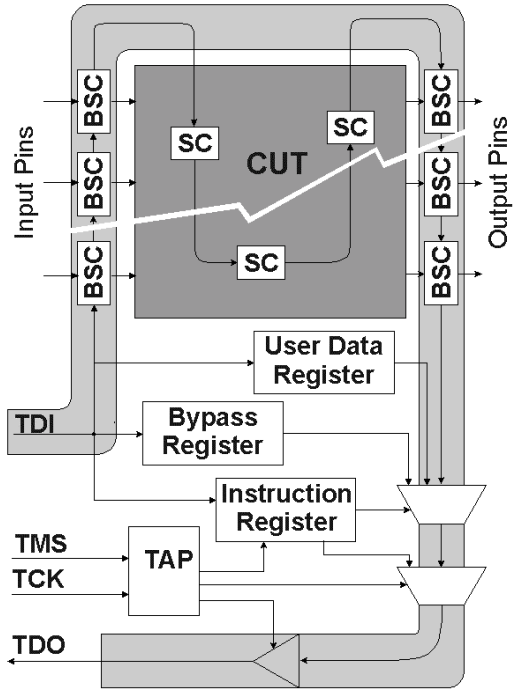


Fig. 1. Boundary Scan on IC

The TAP controller can also bypass the IC using the Bypass Register. The described activities are performed in the frame of three types of compulsory instructions: BYPASS, SAMPLE/PRELOAD and EXTEST. Besides the compulsory instructions a set of optional instructions can be included. The BS method minimizes the switching activity of the internal gates of the CUT while shifting because the scan chain FF outputs in the BS cells are gated by a multiplexor [7].

Another situation occurs if we want to have a diagnostic access to internal FFs. These internal FFs can be included into the scan cells (SC) but as the FF outputs are directly connected with the rest of functional logic shifting patterns through the scan chain causes an activity of the combinational part of the circuit. This activity could be in some cases unacceptable. One solution of the circuit activity reduction was proposed in [5]. As the solution is based on gating the FF outputs with the help of a NOR gate it causes an additional delay in critical functional path. A solution of design partitioning and reordering the scan chain was published in [11] and [8]. Another way was shown in [9]. The authors have proposed filtering of the test pattern subsequences generated in a pseudorandom pattern generator, which do not detect faults. This filtering is performed in additional combinational circuits. Using the RAS diagnostic access methodology [1] may be an alternative solution of the described problem. RAS cells are not concatenated in a chain and thus the output activity of the FFs is substantially lower. As the BS is a commonly used standard access method and it is not necessary to minimize power consumption in all the ICs it is useful to design a RAS like circuitry that can be used simultaneously with the BS. This approach was used in [10].

## 3 Design of Modified Boundary Scan (MBS)

In this paper we propose a solution of the scan chain with substantially reduced impact on the CUT during shifting patterns and without any additional gate in the functional path. The main idea of the proposed solution is described in Fig. 2. The diagnostic access scheme consists of internal cells (Fig. 6) and two alternative types of I/O cells (Fig. 4 and Fig. 5). The I/O cells can be used instead of the BS cells in the BS design and the internal cells replace the scan chain cells from the BS design. The MBS scheme is completed with an auxiliary feedback flip-flop chain. After activating the signal RES, the auxiliary flip-flop chain is set to the state with one logical one (the first bit) and all the other flip-flops are set to zero. During pattern loading the logical one is cyclically shifted through the auxiliary chain. The flip-flop with logical one enables test bit loading through the input TDI to the corresponding cell. Simultaneously it enables reading the state of the next cell to the output TDO. The TDI signal is used in the I/O cells for feeding the TDI input, in the part of the scheme corresponding to the internal cells the TDI signal is used for feeding the S input. The inverted TDI signal is used for feeding the R input. These inputs asynchronously set and reset the cell flip-flops. All the auxiliary chain flip-flops in the scheme are in the diagnostic mode clocked with the signal TCK.

If the circuit is in the functional mode, the internal cells work like a D FF without any additional gates in the functional path. A single latch according to the IC designer requirements can substitute this FF. As we have designed all the circuits in the AMS 0.6 μm technology **Chyba! Nenalezen zdroj odkazů.**, and in this technology there is not any latch with Set and Reset available, we have used D FFs with Set and Reset asynchronous inputs instead of simple latches in the cells. The design of the internal cell is given in Fig. 6. The tri-state buffer IT1 is controlled by the RE signal, which is connected with the output of the neighbor auxiliary chain flip-flop output. The internal flip-flop has a Set and Reset asynchronous inputs. These inputs are controlled from the R and S cell inputs. The TAP controller has the same functions as the BS standard TAP controller.

It is possible to use the proposed modified BS design combined with the classical BS design. In this case we use BS cells on the inputs and outputs of the integrated circuit and the internal scan chain is replaced with the part of the

proposed scheme corresponding to the internal RAS cells only. This solution has partially higher power consumption and is less hardware consuming. A set of sequential benchmark circuits from [3] was used for comparison of hardware overhead of BS and modified BS designs.

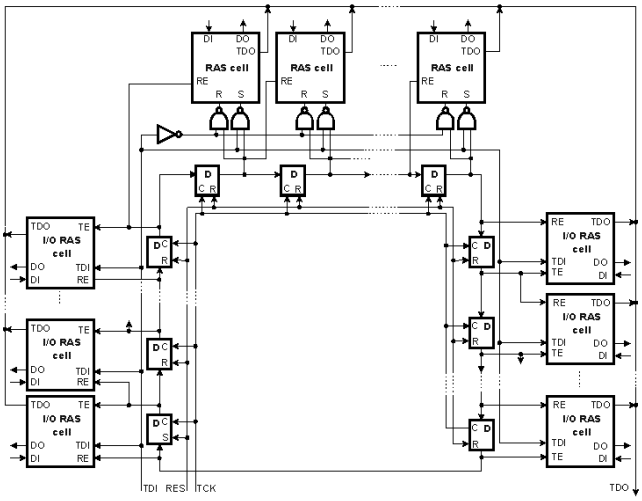


Fig. 2 Proposed MBS diagnostic scheme

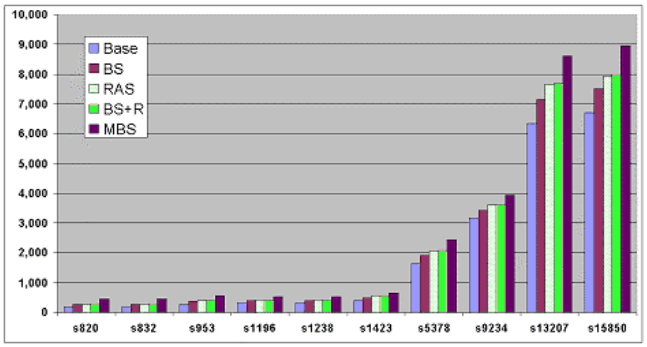


Fig. 3 Hardware overhead (AMS 0.6µm technology **Chyba! Nenalezen zdroj odkazů.**) of ISCAS circuits using standard BS compared with circuits using modified RAS [thousands of µm$^2$].

A comparison of the hardware overhead of these circuits is given in Fig. 3. In the column BASE we have plotted the original area used for the circuit. In the columns BS we have shown the area used for boundary scan design completed with a scan chain. In the columns MBS1 we have plotted the area of the MBS circuits with the reduced I/O cell from Fig. 4.

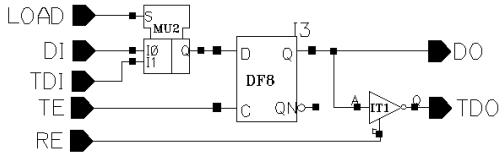


Fig. 4 Reduced I/O cell

The reduced cells (Fig. 4) contain only one flip flop and they are not designed to execute all the BS functions. In column MBS2 we have plotted the area of the MBS circuit with the I/O cells (Fig. 5) fully compatible with the BS design.

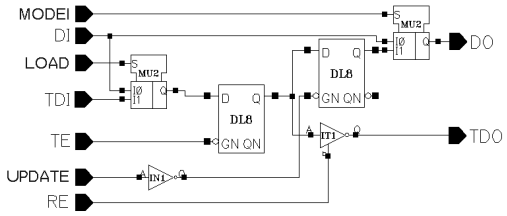


Fig. 5 I/O cell compatible with BS

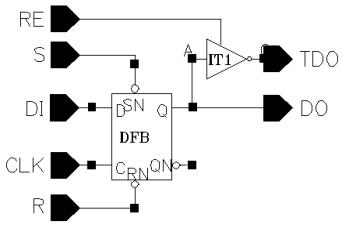


Fig. 6 Internal cell

## 4 Power consumption of BS and MBS

Power dissipation in digital CMOS circuits is divided into static and dynamic one. The static power is comparing to the dynamic one negligible. The average dynamic power of synchronous digital circuits is proportional to the total node transition count (NTC) divided by the number of clock cycles [8]. NTC can be calculated according to the following formula:

$$NTC = \sum_{i \in G} N_{Gi} C_{Gi} + \sum_{i \in FF} (Low_{FFi} + High_{FFi})$$

where $N_{Gi}$ is the total number of gate output transitions (from 0 to 1 and vice versa) for the i-th gate and $C_{Gi}$ is its load capacitance. The load capacitance for each combinational circuit is equal to the number of fan-outs. The sum is done over all combinational gates.

$Low_{FFi}$ is the minimal node transition count of the i-th FF. For MS FFs $Low_{FFi} = 2*\mathrm{Clk_L}$, where $Clk_L$ is the number of clock cycles for which the FF input has the same value as the FF output.

$High_{FFi}$ is the maximal node transition count of the i-th FF. For MS FFs $High_{FFi} = 6*Clk_H$, where $Clk_H$ is the number of clock cycles for which the FF input has different value from the FF output. Let us assume that we have a circuit with 1024 scan chain cells concatenated into a chain and a modified BS circuit with the same number of internal RAS cells. We have calculated the average energy consumed in diagnostic circuitry during loading a test pattern into these circuits. The NTCs of the main parts of the RAS and scan chain diagnostic equipment are given in Tab.1. We can see that the modified BS diagnostic equipment is consuming approx. 77 % of the scan chain energy. In [8] the average values of NTCs per one clock cycle are given for some of the ISCAS circuits. The circuits were tested with test vectors generated by an ATPG ATLANTA [8], without any test vector ordering and compression. In Tab. 2 we demonstrate the CUT

activity during application of the generated test set. In the columns CUT NTC we give average circuit activity during shifting test patterns, we do not consider the activity of the diagnostic circuits and the clock tree. In the column CUT + BS NTC we plot an activity of the whole circuit including the diagnostic circuits and the clock tree.

| | NTC | |
|---|---|---|
| | scan chain | Modyfied scan chain |
| clock tree | 2097152 | 2097152 |
| auxiliary chain | 0 | 2101248 |
| SC/RAS flip-flops | 4194304 | 4096 |
| signal Set | 1024 | 524801 |
| signal Reset | 0 | 524289 |
| TDO | 0 | 512 |
| mpx | 524288 | 0 |
| total NTC | 6291,456 | 565,240 |

Tab. 1 Node transition count of shifting randomly chosen 1024 bites of a scan chain and modyfied BS design.

Comparing the CUT activity, we can see that the percentage of NTC for the modified BS circuit is less than 7 % of the activity of the BS circuit. For circuits with larger number of internal flip-flops this percentage is even smaller. Comparing the total circuit activity during test we can see that for the modified BS circuit design we obtain the NTC equal to max. 24 % of the NTC of the BS circuit. Described MBS design can be combined with power reduction techniques described in [5] and [8].

| | CUT NTC | | | CUT + BS NTC | | |
|---|---|---|---|---|---|---|
| | BS | MBS | % | BS | MBS | % |
| s641 | 116 | 6 | 5 | 166 | 38 | 23 |
| s713 | 121 | 6 | 5 | 173 | 40 | 23 |
| s953 | 111 | 4 | 3 | 158 | 37 | 23 |
| s1196 | 81 | 4 | 6 | 101 | 16 | 15 |
| s1238 | 81 | 4 | 6 | 101 | 16 | 15 |
| s1423 | 313 | 4 | 1 | 453 | 108 | 24 |
| s5378 | 1258 | 7 | 1 | 1772 | 396 | 22 |
| s9234 | 2560 | 11 | 0,4 | 3160 | 463 | 15 |
| s13207 | 4105 | 6 | 0,1 | 5949 | 1 421 | 24 |
| s15850 | 4050 | 8 | 0,2 | 5260 | 932 | 18 |

Tab. 2 Average scan chain and RAS benchmark circuit activity during test given in NTC/number of clock cycles

## 5 Conclusion

As the Random Access Scan has an advantage of consuming lower amount of energy comparing with Boundary Scan we have designed a modified Boundary Scan diagnostic access method, which uses RAS like cells instead of the BS cells. The MBS can be used instead or together with the BS method and it has the same capabilities. If it is used together with the BS, the internal scan chain cells are replaced with the internal MBS cells, the input and output BS cells can be left unchanged. We can resume the advantages and a disadvantage of the proposed method:

- Proposed MBS method has lower power consumption during test in comparison with the BS method combined with the internal flip-flop scan method.
- On the contrary to the BS the proposed MBS method does not add any delay into the functional path of the CUT.
- Hardware overhead of the diagnostic circuitry is greater than that for BS.

For many circuits the greater hardware overhead could be acceptable because of the benefit obtained from the advantages.

## Acknowledgments

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